# NS1081/NS1081S/NS1081Q Datasheet

## USB 3.0 Flash Card Controller

**Revision 1.4**

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**Norelsys**

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# 1. Introduction

NS1081/NS1081S/NS1081Q is a high-performance USB 3.0 Flash Card controller. On one side, it connects with the USB interface and is compatible with USB SuperSpeed (5Gbps), Hi-Speed (480Mbps), and Full-Speed (12Mbps). On the other side, it interfaces with various flash memories, such as Secure Digital (SD), SDHC, SDXC, miniSD, microSD (T-Flash), MultiMediaCard (MMC), Embedded-MultiMediaCard (eMMC), RS-MMC, MMCmicro, or MMCmobile. It also supports high density memory cards with capacity up to 2TB, and high speed memory cards including SD3.0 UHS-I cards and eMMC4.5 HS200.

## 1.1. Highlights

NS1081/NS1081S/NS1081Q integrates self-developed high-performance USB 3.0 transceivers with low-power and low-jitter. The transceivers have built-in test capabilities for guaranteed functions and performance. The IC also integrates high-efficiency regulators, such as 5V to 1.2V DC-DC regulator and 5V to 3.3V/1.8V LDO regulator.

To increase the memory card capacity and data access rate, NS1081 is capable to support 2-channel RAID0 operation, and NS1081Q is capable to support 4-channel RAID0 operation. These innovations are patent pending.

Both NS1081 and NS1081Q are available in 6x6 QFN 48 pin package. NS1081S only supports single-channel memory card. It is available in either 6x6 QFN 48 pin package, which is pin-to-pin compatible to NS1081; or 5x5 QFN 32 pin package, which is used to save the PCB space.

## 1.2. Features

- Support USB 3.0 Specification Revision 1.0.

- USB 3.0 adaptive receiver equalization for better and reliable Super-Speed operation.

- Support USB Specification Revision 2.0.

- Support USB Mass Storage Class, Bulk-Only Transport Specification.

- Support USB 3.0 U0/U1/U2/U3 (P0/P1/P2/P3) and USB 2.0 L0/L1/L2 power saving modes.

- Support Secure Digital v1.0/v1.1/v2.0 SDHC/SDXC (Capacity up to 2TB).

- Support Secure Digital v3.0 UHS-I (Ultra High Speed)：SDR12/SDR25/SDR50/DDR50/SDR104.

- Support MultiMediaCard (MMC) and Embedded MultiMediaCard (eMMC) specification v4.41/v4.5 x1/x4/x8 bit data bus and DDR x4/x8 bit data transfer mode.

- Support Embedded MultiMediaCard (eMMC) specification v4.5 HS200 data transfer mode.

- Built-in variable sampling clock generator to determine correct sampling point for SD UHS card SDR104 mode and eMMC HS200 mode.

- Support user data locking, providing a privacy protection solution.

- Support SD Lock/Unlock Function.

- 25MHz external crystal.

- Support SPI and I2C interface for firmware and Vendor VID/PID customization.

- On-chip high efficiency 5V to 1.2V DC-DC regulator.

- On-chip 5V to 3.3V and 1.8V regulators.

- External Serial Flash memory interface.

- Support ISP（In System Programming）for firmware upgrade to external SPI Flash or I2C EEPROM via USB port.

- On-chip power MOSFETs for supplying flash media card power.

- Support Win8/ Win7/Vista/XP/2000/Me, Linux and Mac OS 9.x/10.x.

- Support two dedicated LED controllers.

- Package available in 48 pin 6x6 (Rohs) QFN or 32 pin 5x5 (Rohs) QFN.

## 2. Pin Locations and Descriptions

### 2.1. NS1081 Package Diagram with Pin Locations

Figure 1 shows the NS1081 pinout from the top of the package.
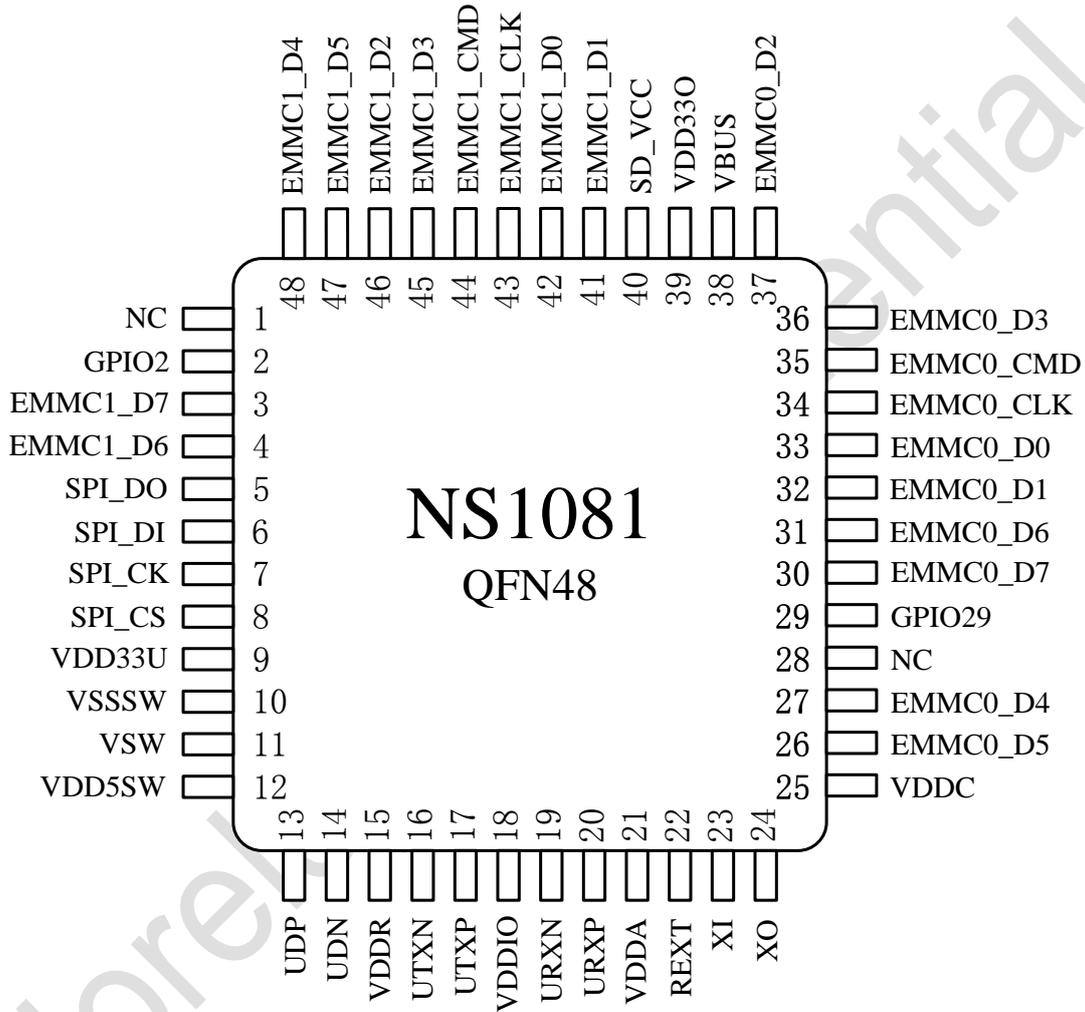


Figure 1. NS1081 48pin QFN package pinout

## 2.2. NS1081S Package Diagram with Pin Locations

Figure 2 shows the NS1081S 48pin package pinout from the top of the package.
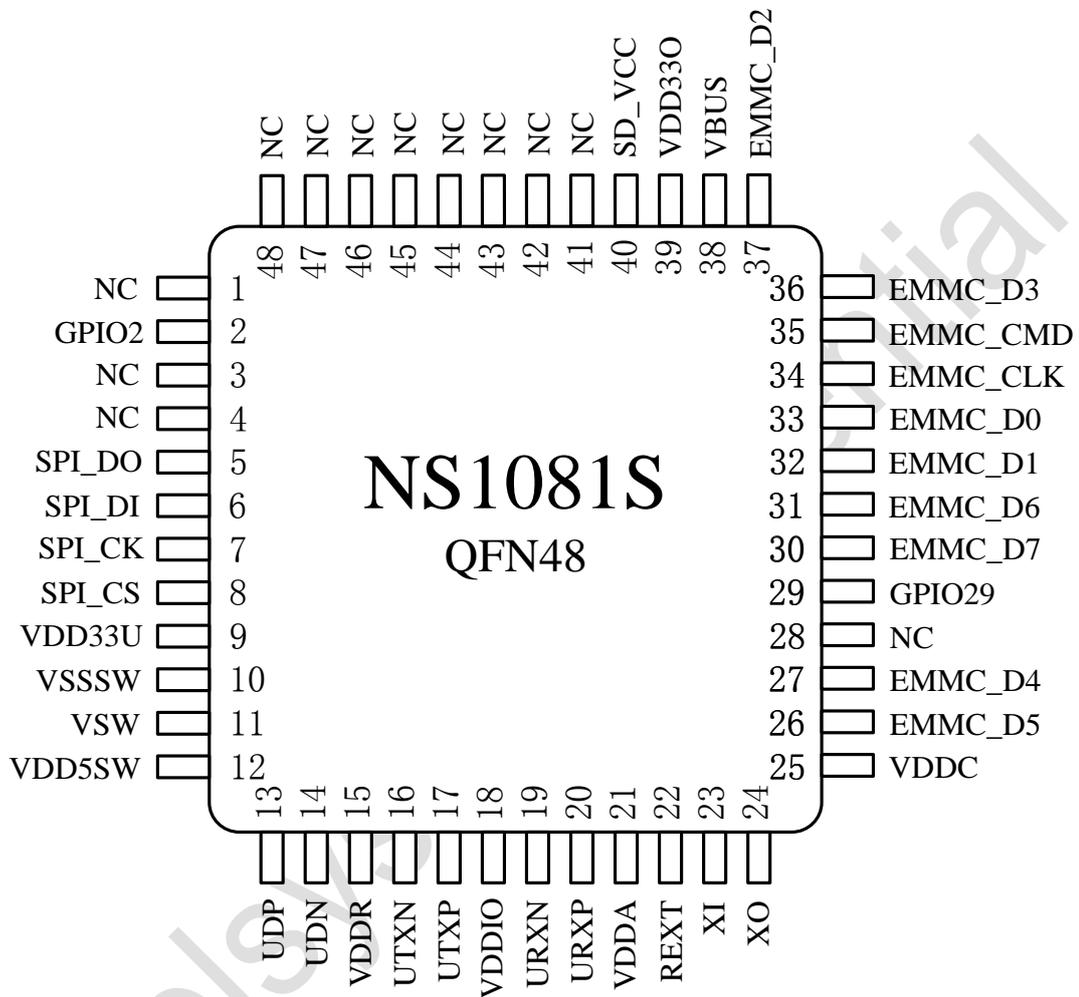


Figure 2. NS1081S 48pin QFN package pinout

Figure 3 shows the NS1081S 32pin package pinout from the top of the package.
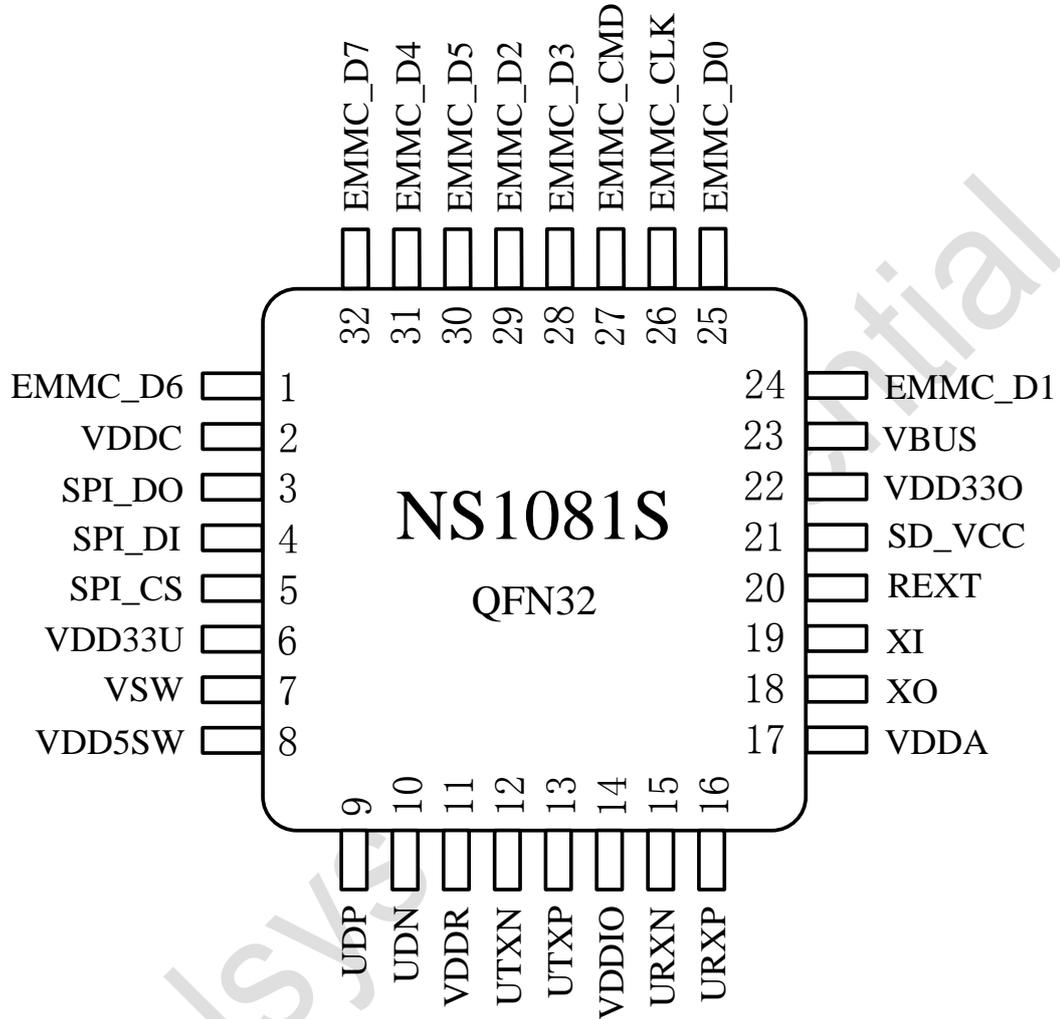
Figure 3. NS1081S 32pin QFN package pinout

## 2.3. NS1081Q Package Diagram with Pin Locations

Figure 4 shows the NS1081Q pinout from the top of the package.
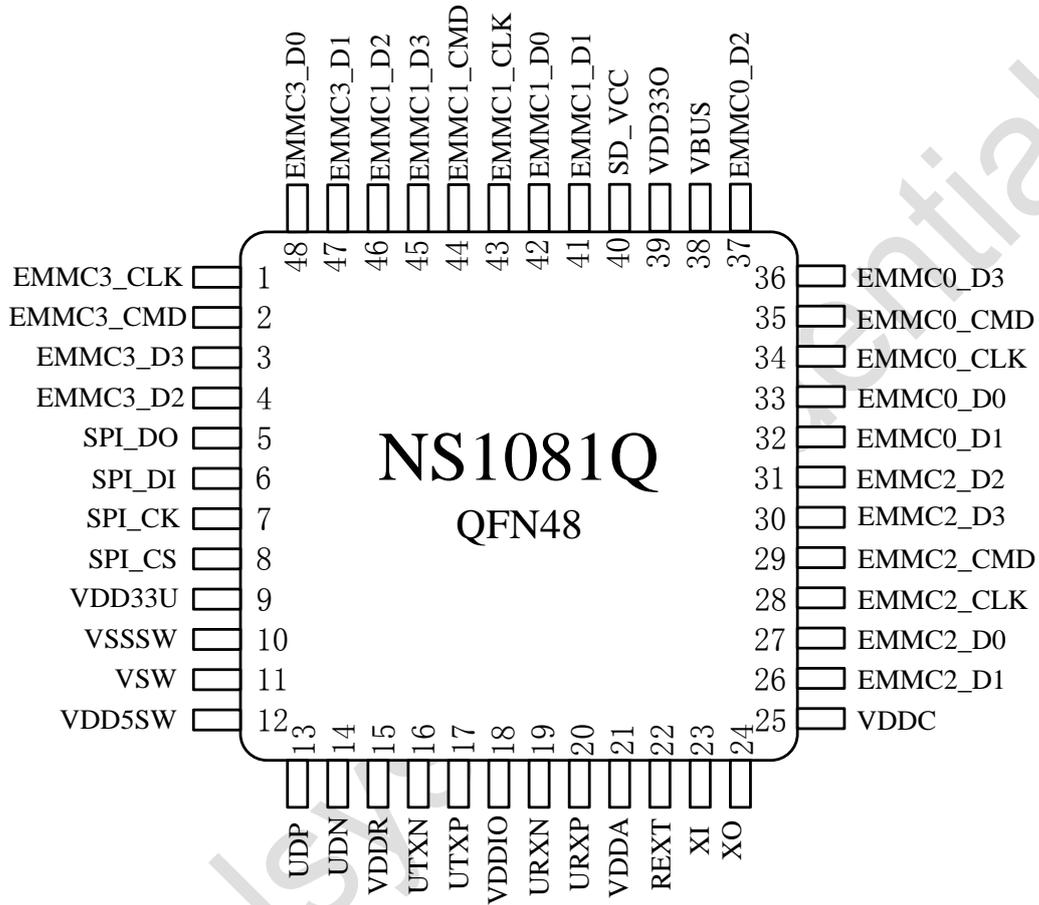


Figure 4. NS1081Q 48pin QFN package pinout

## 2.4. Pin Definitions

This section provides a detailed description of each signal. The signal type is shown in Table 1. Table 2 shows the detailed pin descriptions of both NS1081 and NS1081S. Table 3 shows the detailed pin description of NS1081Q.

Table 1. Pin Type Description

| Type | Description |
|------|-------------|
| I | Input |
| O | Output |
| I/O | Input/output |
| PH | Pull high resistor |
| PL | Pull low resistor |
| P | Power Supply |
| G | Ground |

Table 2. Pin Descriptions of NS1081 and NS1081S

| Signal Name | Pin Number | | | Type | Description |
|-------------|-----------|-----------------|-----------------|------|-------------|
| | NS1081 | NS1081S (QFN48) | NS1081S (QFN32) | | |
| USB3.0 Interface | | | | | |
| URXP | 20 | 20 | 16 | I | USB3.0 RX+ Signal |
| URXN | 19 | 19 | 15 | I | USB3.0 RX- Signal |
| UTXP | 17 | 17 | 13 | O | USB3.0 TX+ Signal A 100nFcapacitor should be connected between this pin and USB connector. |
| UTXN | 16 | 16 | 12 | O | USB3.0 TX- Signal A 100nF capacitor should be connected between this pin and USB connector. |
| USB2.0 Interface | | | | | |
| UDN | 14 | 14 | 10 | I/O | USB2.0 Bus D- Signal |
| UDP | 13 | 13 | 9 | I/O | USB2.0 Bus D+ Signal |
| VBUS | 38 | 38 | 23 | I | USB Cable Power Detector. |
| Flash Card Interface | | | | | |
| EMMC0_CLK | 34 | 34 | - | O | EMMC0 clock output. |
| EMMC0_CMD | 35 | 35 | - | IO | EMMC0 command and response |
| EMMC0_D0 | 33 | 33 | - | IO | EMMC0 data bit0 |

Pin Descriptions of NS1081 and NS1081S (continued)

| | | | | | |
|---|---|---|---|---|---|
| EMMC0_D1 | 32 | 32 | - | IO | EMMC0 data bit1 |
| EMMC0_D2 | 37 | 37 | - | IO | EMMC0 data bit2 |
| EMMC0_D3 | 36 | 36 | - | IO | EMMC0 data bit3 |
| EMMC0_D4 | 27 | 27 | - | IO | EMMC0 data bit4 |
| EMMC0_D5 | 26 | 26 | - | IO | EMMC0 data bit5 |
| EMMC0_D6 | 31 | 31 | - | IO | EMMC0 data bit6 |
| EMMC0_D7 | 30 | 30 | - | IO | EMMC0 data bit7 |
| EMMC1_CLK | 43 | - | 26 | O | EMMC1 clock output. |
| EMMC1_CMD | 44 | - | 27 | IO | EMMC1 command and response |
| EMMC1_D0 | 42 | - | 25 | IO | EMMC1 data bit0 |
| EMMC1_D1 | 41 | - | 24 | IO | EMMC1 data bit1 |
| EMMC1_D2 | 46 | - | 29 | IO | EMMC1 data bit2 |
| EMMC1_D3 | 45 | - | 28 | IO | EMMC1 data bit3 |
| EMMC1_D4 | 48 | - | 31 | IO | EMMC1 data bit4 |
| EMMC1_D5 | 47 | - | 30 | IO | EMMC1 data bit5 |
| EMMC1_D6 | 4 | - | 1 | IO | EMMC1 data bit6 |
| EMMC1_D7 | 3 | - | 32 | IO | EMMC1 data bit7 |
| Crystal Interface | | | | | |
| XI | 23 | 23 | 19 | I | Crystal Input/Oscillator Input. This pin should be connected to a 25MHz crystal or crystal oscillator. |
| XO | 24 | 24 | 18 | O | Crystal Output. If a crystal oscillator connected to XI, XO must be left open. |
| Control and GPIO Interface | | | | | |
| SPI_DO | 5 | 5 | 3 | IO | SPI data output / I2C data |
| SPI_DI | 6 | 6 | 4 | IO | SPI data input / LED0 |
| SPI_CK | 7 | 7 | - | IO | SPI clock output / I2C clock / LED1 |
| SPI_CS | 8 | 8 | 5 | IO | SPI active-low enable |
| REXT | 22 | 22 | 20 | I | $511\,\Omega \pm 1\%$ external reference resistor connected between this pin and VDDIO. |
| GPIO2 | 2 | 2 | - | IO | GPIO2 |
| GPIO29 | 29 | 29 | - | IO | GPIO29 |
| Power and Ground | | | | | |
| VDDA | 21 | 21 | 17 | P | 1.2V Analog Power Supply. |
| VDDR | 15 | 15 | 11 | P | 1.2V Digital Power Supply. |
| VDDC | 25 | 25 | 2 | P | 1.2V Core Logic Power Supply. |

Pin Descriptions of NS1081 and NS1081S (continued)

| VDDIO | 18 | 18 | 14 | P | 1.2V I/O Power Supply. |
|---|---|---|---|---|---|
| VDD33U | 9 | 9 | 6 | P | 3.3V USB2.0 Power Supply. |
| VDD33O | 39 | 39 | 22 | P | 3.3V voltage LDO output. |
| SD_VCC | 40 | 40 | 21 | P | 3.3V card power output. |
| VDD5SW | 12 | 12 | 8 | P | 5V voltage regulator Power Supply. |
| VSW | 11 | 11 | 7 | P | 1.2V voltage regulator output. |
| VSSSW | 10 | 10 | - | G | Voltage regulator Ground. |

Table 3. Pin Description of NS1081Q

| Signal Name | Pin Number | Type | Description |
|---|---|---|---|
| USB3.0 Interface | | | |
| URXP | 20 | I | USB3.0 RX+ Signal |
| URXN | 19 | I | USB3.0 RX- Signal |
| UTXP | 17 | O | USB3.0 TX+ Signal.<br>A 100nFcapacitor should be connected between this pin and USB connector. |
| UTXN | 16 | O | USB3.0 TX- Signal.<br>A 100nF capacitor should be connected between this pin and USB connector. |
| USB2.0 Interface | | | |
| UDN | 14 | I/O | USB2.0 Bus D- Signal |
| UDP | 13 | I/O | USB2.0 Bus D+ Signal |
| VBUS | 38 | I | USB Cable Power Detector. |
| Flash Card Interface | | | |
| EMMC3_CLK | 1 | O | EMMC3 clock output. |
| EMMC3_CMD | 2 | IO | EMMC3 command and response |
| EMMC3_D3 | 3 | IO | EMMC3 data bit3 |
| EMMC3_D2 | 4 | IO | EMMC3 data bit2 |
| EMMC3_D1 | 47 | IO | EMMC3 data bit1 |
| EMMC3_D0 | 48 | IO | EMMC3 data bit0 |
| EMMC2_CLK | 28 | O | EMMC2 clock output. |
| EMMC2_CMD | 29 | IO | EMMC2 command and response |
| EMMC2_D3 | 30 | IO | EMMC2 data bit3 |
| EMMC2_D2 | 31 | IO | EMMC2 data bit2 |
| EMMC2_D1 | 26 | IO | EMMC2 data bit1 |
| EMMC2_D0 | 27 | IO | EMMC2 data bit0 |

Pin Description of NS1081Q (continued)

| | | | |
|---|---|---|---|
| EMMC1_CLK | 43 | O | EMMC1 clock output. |
| EMMC1_CMD | 44 | IO | EMMC1 command and response |
| EMMC1_D3 | 45 | IO | EMMC1 data bit3 |
| EMMC1_D2 | 46 | IO | EMMC1 data bit2 |
| EMMC1_D1 | 41 | IO | EMMC1 data bit1 |
| EMMC1_D0 | 42 | IO | EMMC1 data bit0 |
| EMMC0_CLK | 34 | O | EMMC0 clock output. |
| EMMC0_CMD | 35 | IO | EMMC0 command and response |
| EMMC0_D3 | 36 | IO | EMMC0 data bit3 |
| EMMC0_D2 | 37 | IO | EMMC0 data bit2 |
| EMMC0_D1 | 32 | IO | EMMC0 data bit1 |
| EMMC0_D0 | 33 | IO | EMMC0 data bit0 |
| Crystal Interface | | | |
| XI | 23 | I | Crystal Input/Oscillator Input. This pin should be connected to a 25MHz crystal or crystal oscillator. |
| XO | 24 | O | Crystal Output. If a crystal oscillator connected to XI, XO must be left open. |
| Control and GPIO Interface | | | |
| SPI_DO | 5 | IO | SPI data output / I2C data |
| SPI_DI | 6 | IO | SPI data input / LED0 |
| SPI_CK | 7 | IO | SPI clock output / I2C clock / LED1 |
| SPI_CS | 8 | IO | SPI active-low enable |
| REXT | 22 | I | 511 $\Omega \pm 1\%$ external reference resistor connected between this pin and VDDIO. |
| Power and Ground | | | |
| VDDA | 21 | P | 1.2V Analog Power Supply. |
| VDDR | 15 | P | 1.2V Digital Power Supply. |
| VDDC | 25 | P | 1.2V Core Logic Power Supply. |
| VDDIO | 18 | P | 1.2V I/O Power Supply. |
| VDD33U | 9 | P | 3.3V USB2.0 Power Supply. |
| VDD33O | 39 | P | 3.3V voltage LDO output. |
| SD_VCC | 40 | P | 3.3V card power output. |
| VDD5SW | 12 | P | 5V voltage regulator Power Supply. |
| VSW | 11 | P | 1.2V voltage regulator output. |
| VSSSW | 10 | G | Voltage regulator Ground. |

# 3. Block Diagram and Descriptions

## 3.1. Block Diagram
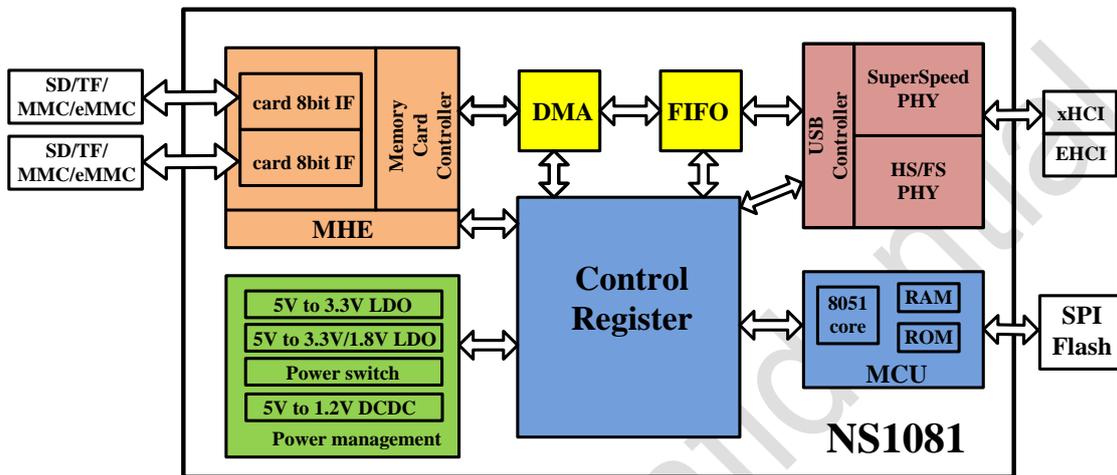


Figure 5. NS1081 Functional Block Diagram
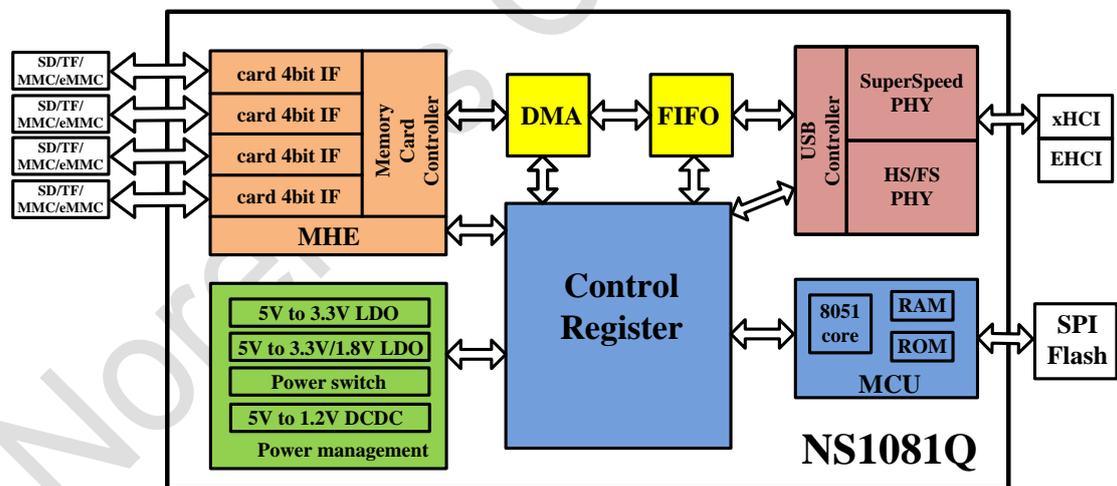


Figure 6. NS1081Q Functional Block Diagram
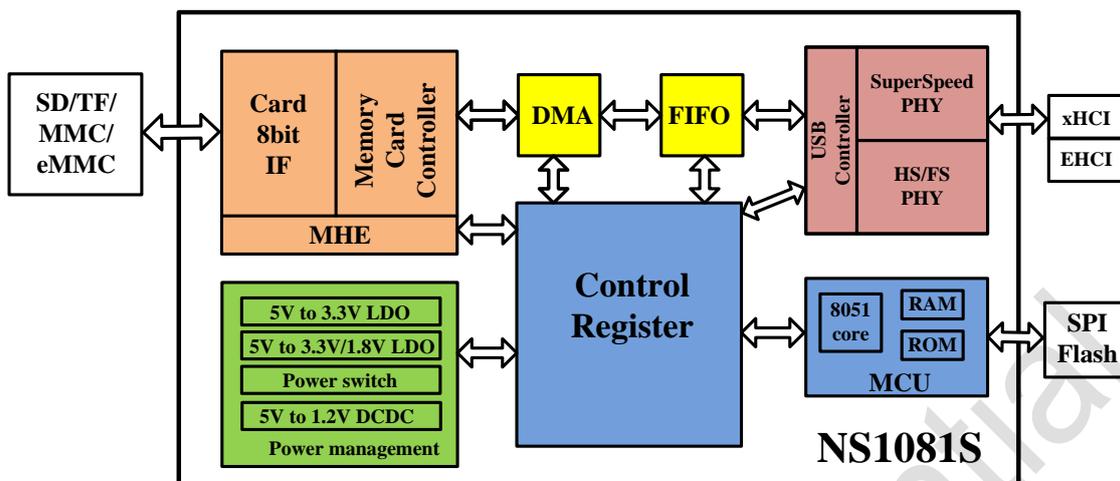
Figure 7. NS1081S Functional Block Diagram

## 3.2. Descriptions

■ **SuperSpeed and HS/FS PHY**

The SuperSpeed and HS/FS PHY contains the transmitter and receiver analog circuitry that handles the low level USB protocol and signaling. The transceivers have built-in test capabilities for guaranteed functions and performance. It also has the function of adaptive receiver equalization for better and reliable Super-Speed operation.

■ **USB Controller**

The usb controller, which contains the logic to handle link layer and protocol layer functions. It also contains various state machines to manage usb packets and transactions.

■ **MHE (Media Hardware Engine)**

Media Interface compatible with SD/TF/MMC/eMMC. It also has the analog circuitry to support both the SDR and DDR data transfer modes.

■ **MCU**

–  **8051 Core**       A fast 8-bit microcontroller which executes ASM51 instruction set.

–  **ROM**            Firmware code on ROM.

–  **RAM**            Program RAM and Data RAM for 8051 Core.

■ **DMA**

The DMA module is integrated in the usb controller and memory card controller. It is used to transfer large chunks of data without MCU intervention. The transfer type and length are configurable.

■ **FIFO**

The FIFO is designed to provide a simple and powerful interface to the on-chip buffer memory for USB controller and memory card controller.

■ **Power Management**

**5V to 3.3V LDO:** current capability 500mA

**5V to 1.2V DCDC:** high-efficiency PWM and PFM for active and suspend mode, respectively

**5V to 3.3V/1.8V LDO:** card IO power, support suspend mode

**Power switch:** support card power off

# 4. Electrical Characteristics

## 4.1. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| VDDA/VDDR/VDDC /VDDIO | 1.2V supply voltage | -0.3 to 1.54 | V |
| VDD33O/VDD33U | 3.3V supply voltage | -0.3 to 4.0 | V |
| VDD5SW | 5V supply voltage | -0.3 to 5.5 | V |
| Storage temperature | $T_{STORAGE}$ | -40 to 150 | ℃ |

## 4.2. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

| Symbol | Parameter | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| VDDA/VDDR/VDDC /VDDIO | 1.2V supply voltage | 1.14 | 1.2 | 1.35 | V |
| VDD33O/VDD33U | 3.3V supply voltage | 3.0 | 3.3 | 3.6 | V |
| VDD5SW | 5V supply voltage | 4.5 | 5 | 5.5 | V |
| $T_A$ | Operating free-air temperature range | 0 | - | 95 | ℃ |
| $T_J$ | Operating junction temperature range | -40 | - | 125 | ℃ |

## 4.3. Reference Clock Requirement

Table 6. Reference Clock Requirement

| Parameter | Min | Type | Max | Unit |
|---|---|---|---|---|
| Crystal frequency | - | 25 | - | MHz |
| Clock Duty Cycle | 45 | 50 | 55 | % |
| Clock frequency accuracy | -300 | | 300 | ppm |

## 4.4. DC Characteristics for Digital IO

Table 7. DC Characteristics for Digital IO

| Symbol | Parameter | Min | Type | Max | Unit |
|--------|-----------|-----|------|-----|------|
| $V_{IH}$ | Input High Lever | 2.0 | - | 3.6 | V |
| $V_{IL}$ | Input Low Lever | - | - | 0.8 | V |
| $V_{OH}$ | Output High Level | 2.4 | - | - | V |
| $V_{OL}$ | Output Low Level | - | - | 0.5 | V |
| $I_{ACTIVE}$ | Super Speed Mode | | 132 | | mA |
| | High-Speed Mode | | 55.0 | | mA |
| $I_{SUSPEND}$ | Super Speed Mode | | 1.53 | | mA |
| | High-Speed Mode | | 1.66 | | mA |

## 4.5. Power Up and Reset Timing

The Power Up and Reset Timing rules are defined in this section. Designers should follow all the rules for external power designs. Detailed explanations are listed as Figure 8.
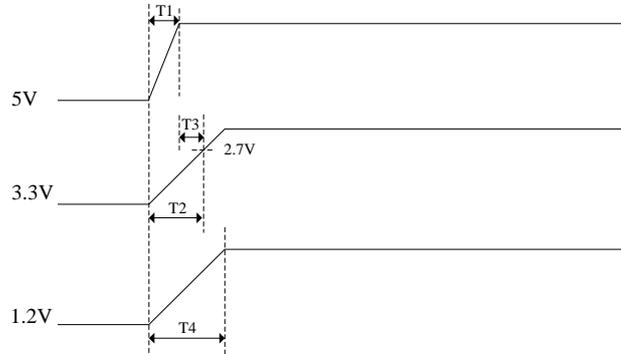


Figure 8. Power Up and Reset Timing

T1: Rise time for 5V power rail form 0V to 5V

T2: Rise time for 3.3V power rail form 0V to 2.7V

T3: Delay from the time when 5V power is ready to the time when 3.3V power supply voltage reaches 2.7V.

T4: Rise time for 1.2V power rail form 0V to 1.2V

The recommended power sequence and timing requirements are listed as Table 8.

Table 8. Power Up and Reset Timing Requirement

| Time | Min | Max |
|------|-----|-----|
| T1 | 0.01ms | 1ms |
| T2 | 0.01ms | 1ms |
| T3 | 0.01ms | 0.2ms |
| T4 | 0.01ms | 1ms |

# 5. Package Information

## 5.1. 48 pin QFN (6x6) package

Figure 9. 48 pin QFN package outline
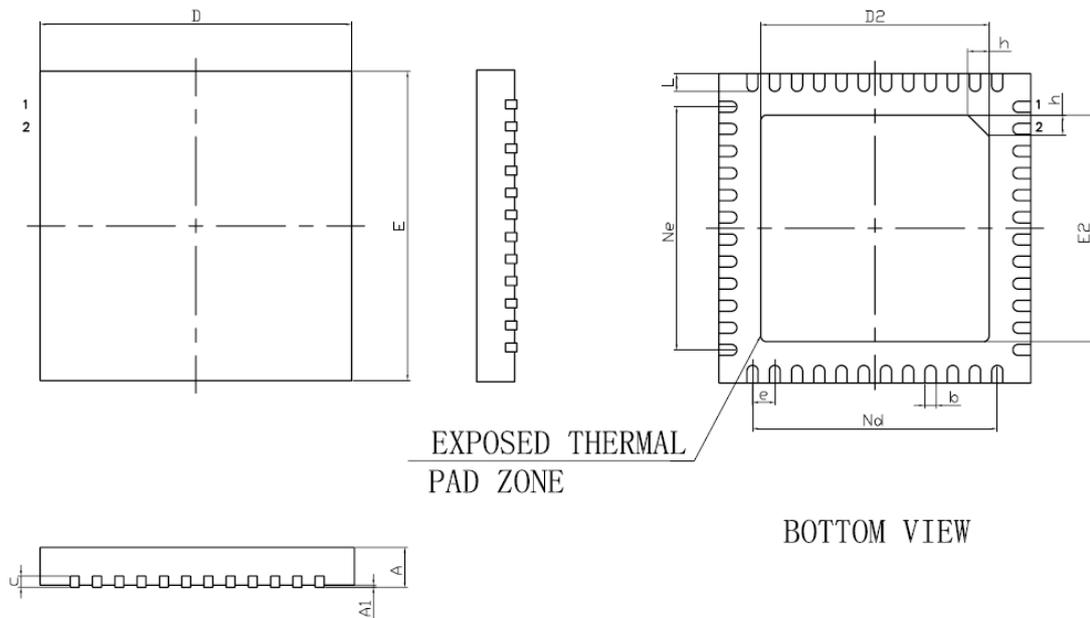


Table 9. 48 pin QFN package mechanical data

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.23 |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 4.10 | 4.20 | 4.30 |
| e | 0.40BSC | | |
| Ne | 4.40BSC | | |
| Nd | 4.40BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 4.10 | 4.20 | 4.30 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 (MIL) | 177*177 | | |

## 5.2. 32 pin QFN (5x5) package

Figure 10. 32 pin QFN package outline
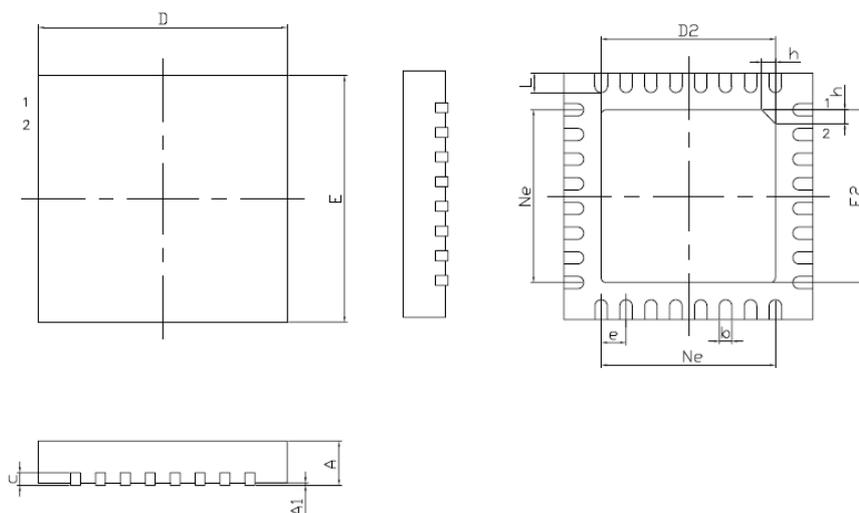


Table 10. 32 pin QFN package mechanical data

| SYMBOL | MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | — | 0.05 |
| b | 0.18 | 0.30 |
| c | 0.18 | 0.25 |
| D | 4.90 | 5.10 |
| D2 | 3.40 | 3.60 |
| e | 0.50BSC | |
| Ne | 3.50BSC | |
| E | 4.90 | 5.10 |
| E2 | 3.40 | 3.60 |
| L | 0.35 | 0.45 |
| h | 0.30 | 0.40 |