ZOOM FAMILY

SM2246XT

SATA Solid-State Drive Controller

Datasheet

Revision 0.7 **Aug 2015**

Revision History

Revision	Date	Description
0.1	Aug 27, 2013	Preliminary release
0.2	Oct 4, 2013	Renamed the signals and updated the Ball Assignments: A15, C15, E11, E12, E13, F6, F7, F8, F9, F10, F11, and G17 (2.1 and 2.2)
0.3	Jan 14, 2014	• Updated the features of flash memory support (1.2) • Added the BGA-144 ball assignments and package outline (2.1, 2.2, and 5.2) • Updated the QFN-88 ball assignments and the pin name of pin No. 3 (2.1) (2.3) • Added SM2246XT package pin list (2.2) • Updated flash and miscellaneous signal descriptions (2.3) • Updated minor text descriptions
0.4	Mar 14, 2014	• Updated the miscellaneous signal types: GPIO2[6] and GPIO2[7] (2.3) • Updated Identify Device Data (4.2.1) and added Identify Device data of CFast Mode (4.2.2) • Updated SMART Data Structure (4.3.1) and SMART Attributes (4.3.2) • Added the TFBGA-144 top marking (5.4) and ordering information (6)
0.5	Sep 30, 2014	• Updated NAND Flash Support feature (1.2) • Updated Block Diagram (1.4) • Fixed the signal type of flash chip enable and updated the signal description of GPIO1[2] (2.3)
0.6	Nov 11, 2014	• Added new ordering numbers SM224ME0600XT-XX, SM224HE0600XT-XX and the top markings (Figure 13)(Figure 14)(Table 23) • Updated the DC Characteristics of VCCGQ (Table 6) • Updated the DC Characteristics of 3.3V and 1.8V I/O pins (Table 8)(Table 9)
0.7	Aug 27, 2015	• Updated signal descriptions of GPIO1[0], GPIO1[2], GPIO1[3] and GPIO1[5] (2.3)

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Table of Contents

1. Overview 7
1.1 Product Description 7
1.2 Key Features 7
1.3 Functional Description 9
1.4 Block Diagram 10
2. Signal Descriptions 11
2.1 Pin Assignments 11
2.2 SM2246XT Package Pin List 14
2.3 Signal Descriptions 19
3. Electrical Characteristics 25
3.1 DC Characteristics 25
3.2 Flash Interface AC Characteristics 28
3.2.1 Legacy NAND (SDR) Interface 28
3.2.2 NV-DDR Interface 31
4. Software Interface 36
4.1 Command Set 36
4.2 Identify Device Information 38
4.2.1 Identify Device - SATA 38
4.2.2 Identify Device - CFast 41
4.3 SMART Feature Set 44
4.3.1 SMART Data Structure 45
4.3.2 SMART Attributes 47
4.4 Capacity 48
5. Package Information 49
5.1 88-Pin QFN Package 49
5.2 144-Ball TFBGA Package 50
5.3 288-Ball TFBGA Package 51
5.4 Top Marking 52
6. Product Ordering Information 54

List of Tables

Table 1: Pin List 14
Table 2: Flash Interface Signals 19
Table 3: SATA Interface Signals 21
Table 4: Power Signals 21
Table 5: Miscellaneous Signals 23
Table 6: Recommended Operating Conditions 25
Table 7: Operating Temperature 25
Table 8: General DC Characteristics for 3.3V I/O Interface 26
Table 9: General DC Characteristics for 1.8V I/O Interface 26
Table 10: Power-on Reset 26
Table 11: Host Voltage Detection 27
Table 12: Flash Voltage Detection 27
Table 13: PLL 27
Table 14: Flash Interface AC Characteristics for Legacy NAND 28
Table 15: Flash Interface AC Characteristics for NV-DDR 31
Table 16: Command Set 36
Table 17: Identify Device Data of General SATA Mode 38
Table 18: Identify Device Data of CFast Mode 41
Table 19: SMART Feature Register Values 44
Table 20: SMART Data Structure 45
Table 21: SMART Data Vendor-specific Attributes 47
Table 22: Capacity Information 48
Table 23: Ordering Information 54

List of Figures

Figure 1: SM2246XT Block Diagram 10
Figure 2: 88-Pin QNF Assignments (Top View) 11
Figure 3: 144-Ball TFBGA Assignments (Top View – Balls Down) 12
Figure 4: 288-Ball TFBGA Assignments (Top View – Balls Down) 13
Figure 5: Command Latch Timing 29
Figure 6: Address Latch Timing 29
Figure 7: Data Output (Write) Cycle Timing 30
Figure 8: Data Input (Read) Cycle Timing 30
Figure 9: NV-DDR Command Cycle Timing 32
Figure 10: NV-DDR Address Cycle Timing 33
Figure 11: NV-DDR Data Output (Write) Cycle Timing 34
Figure 12: NV-DDR Data Input (Read) Cycle Timing 35
Figure 13: 88-Pin QFN Top Marking Information 52
Figure 14: 144-Ball TFBGA Top Marking Information 52
Figure 15: 288-Ball TFBGA Top Marking Information 53

1. Overview

1.1 Product Description

The SM2246XT is a high-performance SATA 6Gb/s SSD controller ideally suited for both client SSDs as well as NAND-cache drives used in performance-enhancing hybrid storage solutions for PCs, Ultrabooks, Tablet PCs, and other embedded applications.

The single-chip, DRAM-less design fits in smaller form factor with reduced BOM cost, and without impacting performance. Its ultra-low power consumption effectively extends battery life and optimizes user experience. The SM2246XT fully supports the latest generation NAND in high-speed Toggle, ONFI, or Async mode, enabling the realization of high capacity and highly reliable SSDs on the market.

1.2 Key Features

- Host Interface
  - Industrial Standard SATA Revision 3.1 compliant
  - Industrial Standard ATA/ATAPI-8 and ACS-2 command compliant
  - Supports SATA interface rate of 6Gb/s (backward compatible to 1.5Gb/s and 3Gb/s)
  - Native Command Queuing up to 32 commands
  - SATA Device Sleep (DevSleep)
  - Data Set Management command (TRIM)
  - Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
  - Supports PHY Sleep mode (CFast PHYSLP)
  - Supports 28-bit and 48-bit LBA (Logical Block Addressing) mode commands
- NAND Flash Support
  - Supports 1x/1y/2x/2y/3xnm SLC and MLC
  - Supports ONFI 3.0[1], Toggle 2.0 interface, and Asynchronous interface
  - Supports 1.8V/3.3V flash I/O
  - Supports 8KB and 16KB page size
  - Supports 1-plane, 2-plane, and 4-plane operation
  - 4-/2-channel flash interface supports up to 32 NAND flash devices
- Data Protection and Reliability
  - Supports ATA8 security feature set
  - Supports data security erase and quick erase
  - Hardware BCH ECC capable of correcting errors up to 66-bit/1KB
  - Internal data shaping technique increases data endurance

[1] ONFI NV-DDR2 and Toggle DDR 2.0 NAND are supported in the 288-BGA package only.

- Data Protection and Reliability
  - Software/Hardware write protect option
  - StaticDataRefresh technology ensures data integrity
  - Early weak block retirement option
  - Global wear leveling algorithm evens program/erase count and maximizes SSD lifespan
- Architecture
  - 32-bit RISC CPU
  - High-efficiency 64-bit system bus
  - Automatic sleep and wake-up mechanism to save power
  - Built-in voltage detectors for power failure protection
  - Built-in power-on reset and voltage regulators
  - Built-in temperature sensor for SSD temperature detection
  - Supports JTAG interface, UART (RS-232) interface, and I^2C interface for on-system debug
- Upgradeable Firmware
  - Supports firmware in-system programming (ISP) function for firmware upgrade
- High Performance
  - Sequential Read: up to 530 MB/s (synchronous mode)
  - Sequential Write: up to 410 MB/s (synchronous mode)
- Operating Temperature
  - Commercial Grade: 0°C ~ 70°C
  - Industrial Grade: -40°C ~ +85°C
- Package Options (Lead-free and RoHS compliant)
  - 88-pin QFN: 2-channel flash interface supports up to 4 NAND flash devices
  - 144-ball TFBGA: 4-channel flash interface supports up to 16 NAND flash devices
  - 288-ball TFBGA: 4-channel flash interface supports up to 32 NAND flash devices

1.3 Functional Description

Host Interface

The high-speed SATA interface is compliant with SATA Revision 3.1 and ATA-8 ACS-2 specifications, and supports CFast PHYSLP and SATA DEVSLP to greatly save power consumption.

Flash Interface and Data Transfer

The flash interface enables 2-way and 4-way interleaving for a multi-bank NAND flash connection to obtain optimal performance. The SM2246XT uses a superior DMA technology to transfer data between the host and the NAND flash interface. The DMA technology transfers data at a very high rate in both directions (read and write) and in doing so, effectively decreases the loading of micro processor.

Flash Memory Support and Error Management

The SM2246XT fully supports high-speed Toggle, ONFI, and legacy Asynchronous NAND. The hardware Error Correction Coding (ECC) engine executes parity generation and error detection/ correction features, and enhances decoding throughput and data reliability. With multi-mode correction capability up to 66 bits, the powerful ECC engine is able to support the latest generation NAND.

Data Security

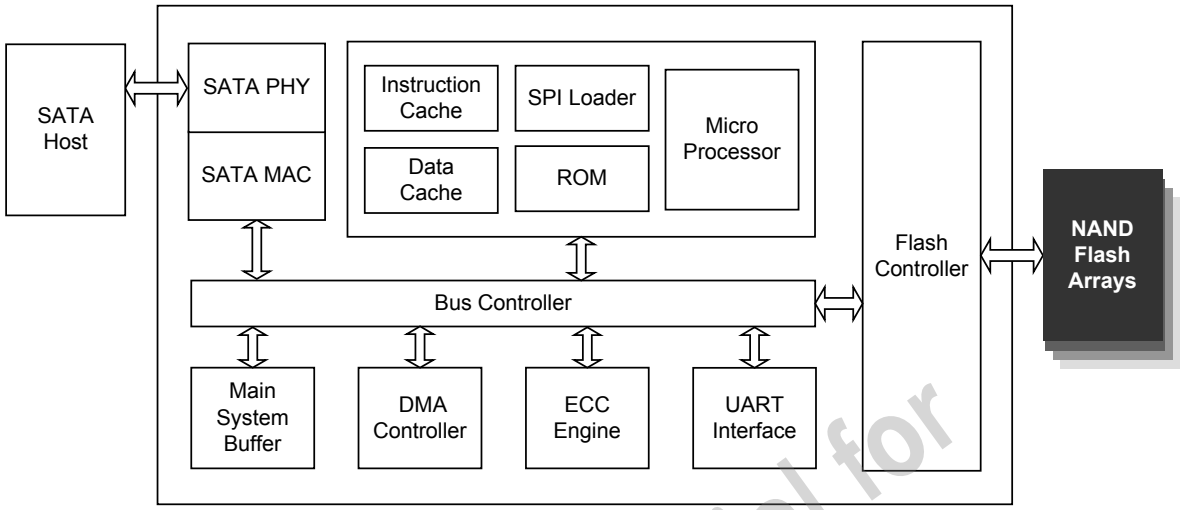
Data security commands can be used to lock and unlock the drive by password or a hardware switch. Customized command is another option for erasing blocks for those users who require a high level of security.

SMART

The SM2246XT supports SMART commands that allow users to read spare and bad block information. The users can thus evaluate drive health at run time and receive an early warning before the drive life ends.

1.4 Block Diagram

Figure 1: SM2246XT Block Diagram



2. Signal Descriptions

2.1 Pin Assignments

Figure 2: 88-Pin QNF Assignments (Top View)

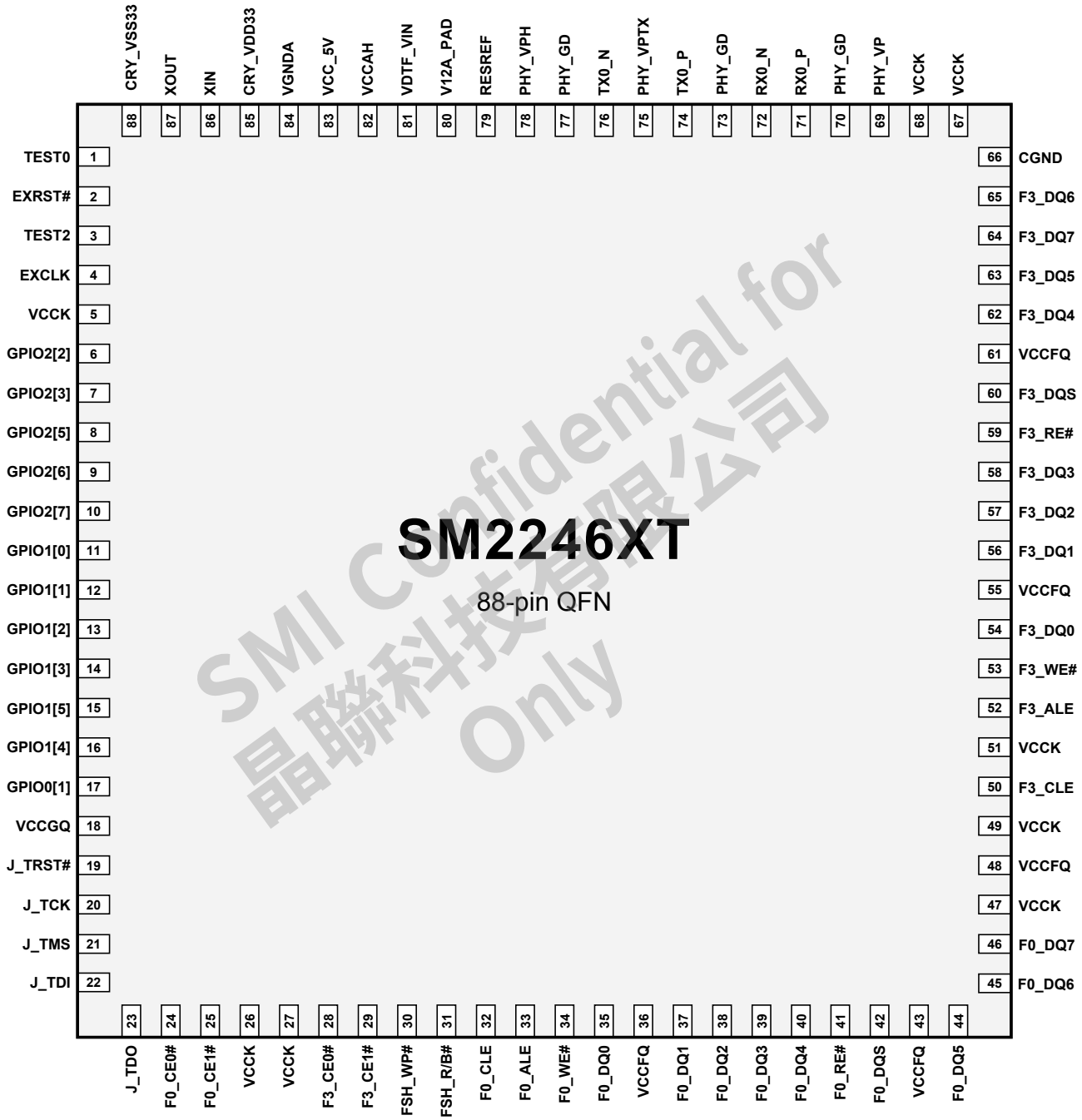
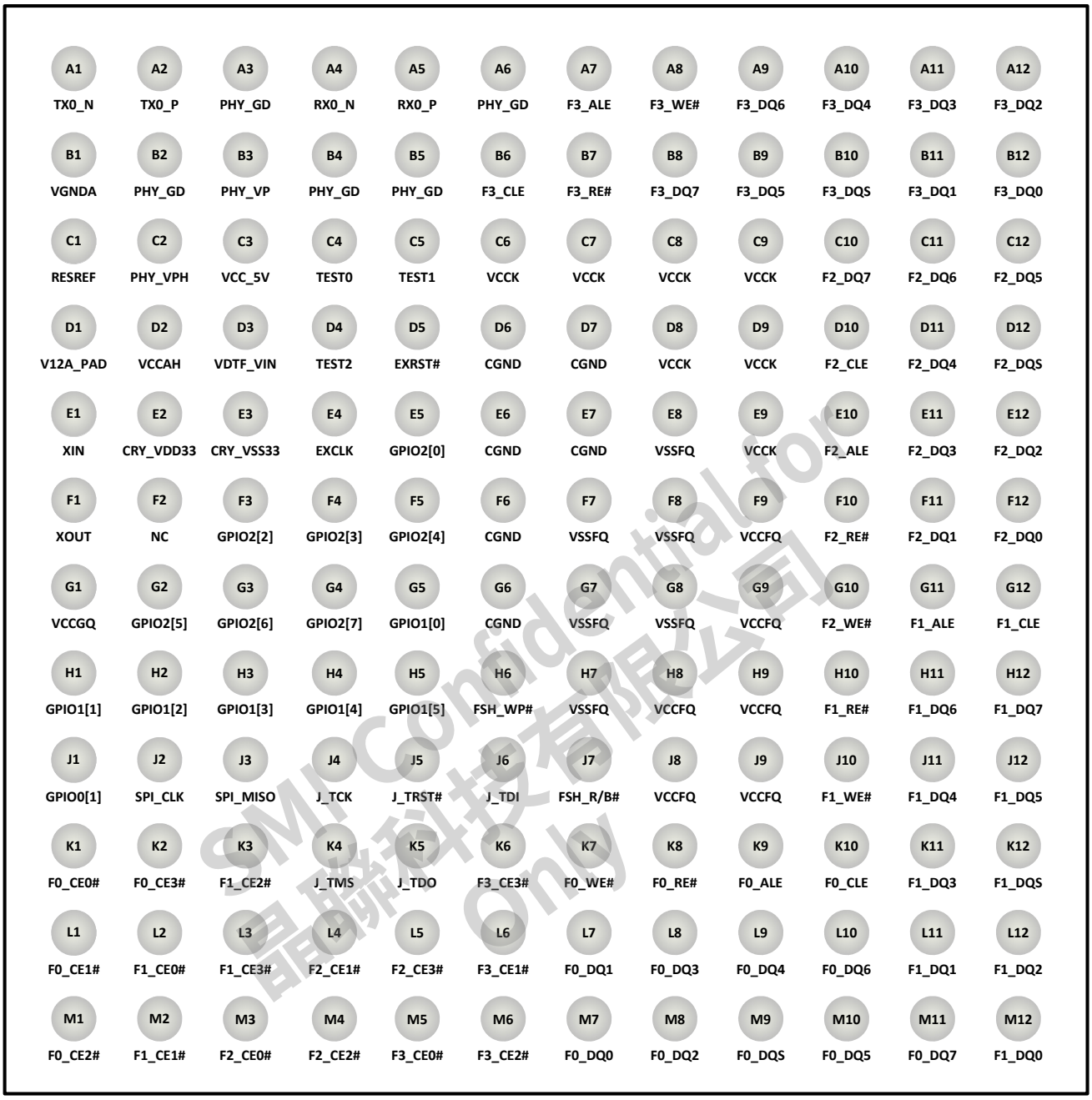


Figure 3: 144-Ball TFBGA Assignments (Top View – Balls Down)



A1 TX0_N	A2 TX0_P	A3 PHY_GD	A4 RX0_N	A5 RX0_P	A6 PHY_GD	A7 F3_ALE	A8 F3_WE#	A9 F3_DQ6	A10 F3_DQ4	A11 F3_DQ3	A12 F3_DQ2
B1 VGNDA	B2 PHY_GD	B3 PHY_VP	B4 PHY_GD	B5 PHY_GD	B6 F3_CLE	B7 F3_RE#	B8 F3_DQ7	B9 F3_DQ5	B10 F3_DQS	B11 F3_DQ1	B12 F3_DQ0
C1 RESREF	C2 PHY_VPH	C3 VCC_5V	C4 TEST0	C5 TEST1	C6 VCCK	C7 VCCK	C8 VCCK	C9 VCCK	C10 F2_DQ7	C11 F2_DQ6	C12 F2_DQ5
D1 V12A_PAD	D2 VCCAH	D3 VDTF_VIN	D4 TEST2	D5 EXRST#	D6 CGND	D7 CGND	D8 VCCK	D9 VCCK	D10 F2_CLE	D11 F2_DQ4	D12 F2_DQS
E1 XIN	E2 CRY_VDD33	E3 CRY_VSS33	E4 EXCLK	E5 GPIO2[0]	E6 CGND	E7 CGND	E8 VSSFQ	E9 VCCK	E10 F2_ALE	E11 F2_DQ3	E12 F2_DQ2
F1 XOUT	F2 NC	F3 GPIO2[2]	F4 GPIO2[3]	F5 GPIO2[4]	F6 CGND	F7 VSSFQ	F8 VSSFQ	F9 VCCFQ	F10 F2_RE#	F11 F2_DQ1	F12 F2_DQ0
G1 VCCGQ	G2 GPIO2[5]	G3 GPIO2[6]	G4 GPIO2[7]	G5 GPIO1[0]	G6 CGND	G7 VSSFQ	G8 VSSFQ	G9 VCCFQ	G10 F2_WE#	G11 F1_ALE	G12 F1_CLE
H1 GPIO1[1]	H2 GPIO1[2]	H3 GPIO1[3]	H4 GPIO1[4]	H5 GPIO1[5]	H6 FSH_WP#	H7 VSSFQ	H8 VCCFQ	H9 VCCFQ	H10 F1_RE#	H11 F1_DQ6	H12 F1_DQ7
J1 GPIO0[1]	J2 SPI_CLK	J3 SPI_MISO	J4 J_TCK	J5 J_TRST#	J6 J_TDI	J7 FSH_R/B#	J8 VCCFQ	J9 VCCFQ	J10 F1_WE#	J11 F1_DQ4	J12 F1_DQ5
K1 F0_CE0#	K2 F0_CE3#	K3 F1_CE2#	K4 J_TMS	K5 J_TDO	K6 F3_CE3#	K7 F0_WE#	K8 F0_RE#	K9 F0_ALE	K10 F0_CLE	K11 F1_DQ3	K12 F1_DQS
L1 F0_CE1#	L2 F1_CE0#	L3 F1_CE3#	L4 F2_CE1#	L5 F2_CE3#	L6 F3_CE1#	L7 F0_DQ1	L8 F0_DQ3	L9 F0_DQ4	L10 F0_DQ6	L11 F1_DQ1	L12 F1_DQ2
M1 F0_CE2#	M2 F1_CE1#	M3 F2_CE0#	M4 F2_CE2#	M5 F3_CE0#	M6 F3_CE2#	M7 F0_DQ0	M8 F0_DQ2	M9 F0_DQS	M10 F0_DQ5	M11 F0_DQ7	M12 F1_DQ0

Figure 4: 288-Ball TFBGA Assignments (Top View – Balls Down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A		TX0_N	TX0_P	PHY_GD	RX0_N	RX0_P	PHY_GD	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	RESREF	PHY_GD	PHY_GD	VCCK	PHY_GD	PHY_GD	VCCK	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	V12A_ PAD	PHY_VPH	PHY_VPH	PHY_ VPTX	PHY_VP	VCCK	VCCK	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D	V12A_ PAD	V18_ PAD	V18_ PAD	VCCAH	VCCK	VCCK	VCCK	NC	NC	NC	NC	NC	NC	NC	NC	VSSFQ	NC
E	XIN	NC	VDTF_ VIN	VCCAH	VCCK	VCCK	VCCK	VCCK	VCCK	NC	NC	NC	NC	NC	NC	NC	NC
F	XOUT	VGNDA	CRY_ VDD33	EXCLK	TEST2	NC	NC	NC	NC	NC	NC	VSSFQ	VSSFQ	VSSFQ	NC	NC	NC
G	VCC_5V	CRY_ VSS33	GPIO2[0]	NC	CGND	CGND	CGND	CGND	CGND	VSSFQ	VSSFQ	VSSFQ	NC	NC	NC	NC	NC
H	VCCGQ	VCCGQ	GPIO2[3]	GPIO2[5]	GPIO1[1]	CGND	CGND	CGND	CGND	CGND	VSSFQ	VSSFQ	NC	NC	NC	NC	NC
J	TEST0	GPIO2[4]	GPIO1[2]	GPIO1[3]	GPIO1[5]	VSSFQ	VSSFQ	CGND	CGND	VSSFQ	VSSFQ	VSSFQ	F3_DQ7	F3_DQ1	F3_DQ4	F3_DQ6	F3_DQ5
K	GPIO2[2]	GPIO1[4]	SPI_CLK	GPIO1[7]	GPIO0[1]	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VCCFQ	VCCFQ	F3_DQ2	F3_DQ0	F3_DQS	F3_DQS#
L	GPIO2[6]	SPI_CS#	J_TDO	SPI_MOSI	CGND	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VCCFQ	VCCFQ	F1_DQ4	F3_ALE	F3_DQ3	F3_RE#	F3_RE
M	EXRST#	SPI_MISO	F0_CE6#	J_TRST#	I2C_SCL	VCCFQ	VCCFQ	VCCFQ	VCCFQ	VCCFQ	VCCFQ	VCCFQ	F1_DQ2	F2_DQ1	F3_CLE	FSH_ VREF	F3_WE#
N	TEST1	I2C_SDA	F0_CE4#	J_TMS	F0_CE2#	F1_CE7#	F2_CE4#	F3_CE2#	F3_CE5#	FSH_ R/B#	F0_DQ1	F0_DQ2	VCCFQ	F1_DQ6	F2_DQ6	F2_DQ5	F2_DQ7
P	GPIO2[7]	J_TCK	F1_CE5#	F0_CE5#	F1_CE1#	F2_CE1#	F2_CE2#	F3_CE3#	FSH_ WP#	F0_ALE	F0_DQ6	F0_DQ7	F1_ALE	F1_DQ5	F2_DQ2	F2_DQ4	F2_DQS#
R	GPIO1[0]	J_TDI	F1_CE2#	F0_CE7#	F2_CE0#	F2_CE5#	F2_CE7#	F3_CE6#	F0_CLE	F0_DQ3	F0_DQ5	F1_CLE	F1_DQ1	F1_DQ3	F2_CLE	F2_DQ0	F2_DQS
T	GPIO1[6]	F0_CE1#	F0_CE3#	F1_CE0#	F1_CE6#	F2_CE6#	F3_CE1#	F3_CE7#	F0_WE#	F0_RE	F0_DQS	F1_DQ0	F1_RE	F1_DQS	F2_WE#	F2_ALE	F2_RE#
U	GPIO0[0]	F0_CE0#	F1_CE3#	F1_CE4#	F2_CE3#	F3_CE0#	F3_CE4#	F0_DQ0	F0_DQ4	F0_RE#	F0_DQS#	F1_WE#	F1_RE#	F1_DQS#	F1_DQ7	F2_DQ3	F2_RE

2.2 SM2246XT Package Pin List

Table 1: Pin List

Signal Name	TFBGA 288	TFBGA 144	QFN 88
F0_DQ0	U8	M7	35
F0_DQ1	N11	L7	37
F0_DQ2	N12	M8	38
F0_DQ3	R10	L8	39
F0_DQ4	U9	L9	40
F0_DQ5	R11	M10	44
F0_DQ6	P11	L10	45
F0_DQ7	P12	M11	46
F1_DQ0	T12	M12	-
F1_DQ1	R13	L11	-
F1_DQ2	M13	L12	-
F1_DQ3	R14	K11	-
F1_DQ4	L13	J11	-
F1_DQ5	P14	J12	-
F1_DQ6	N14	H11	-
F1_DQ7	U15	H12	-
F2_DQ0	R16	F12	-
F2_DQ1	M14	F11	-
F2_DQ2	P15	E12	-
F2_DQ3	U16	E11	-
F2_DQ4	P16	D11	-
F2_DQ5	N16	C12	-
F2_DQ6	N15	C11	-
F2_DQ7	N17	C10	-
F3_DQ0	K15	B12	54
F3_DQ1	J14	B11	56
F3_DQ2	K14	A12	57
F3_DQ3	L15	A11	58
F3_DQ4	J15	A10	62
F3_DQ5	J17	B9	63
F3_DQ6	J16	A9	65
F3_DQ7	J13	B8	64

Signal Name	TFBGA 288	TFBGA 144	QFN 88
F0_ALE	P10	K9	33
F1_ALE	P13	G11	-
F2_ALE	T16	E10	-
F3_ALE	L14	A7	52
F0_CLE	R9	K10	32
F1_CLE	R12	G12	-
F2_CLE	R15	D10	-
F3_CLE	M15	B6	50
F0_CE0#	U2	K1	24
F0_CE1#	T2	L1	25
F0_CE2#	N5	M1	-
F0_CE3#	T3	K2	-
F0_CE4#	N3	-	-
F0_CE5#	P4	-	-
F0_CE6#	M3	-	-
F0_CE7#	R4	-	-
F1_CE0#	T4	L2	-
F1_CE1#	P5	M2	-
F1_CE2#	R3	K3	-
F1_CE3#	U3	L3	-
F1_CE4#	U4	-	-
F1_CE5#	P3	-	-
F1_CE6#	T5	-	-
F1_CE7#	N6	-	-
F2_CE0#	R5	M3	-
F2_CE1#	P6	L4	-
F2_CE2#	P7	M4	-
F2_CE3#	U5	L5	-
F2_CE4#	N7	-	-
F2_CE5#	R6	-	-
F2_CE6#	T6	-	-
F2_CE7#	R7	-	-

Signal Name	TFBGA 288	TFBGA 144	QFN 88
F3_CE0#	U6	M5	28
F3_CE1#	T7	L6	29
F3_CE2#	N8	M6	-
F3_CE3#	P8	K6	-
F3_CE4#	U7	-	-
F3_CE5#	N9	-	-
F3_CE6#	R8	-	-
F3_CE7#	T8	-	-
F0_DQS	T11	M9	42
F0_DQS#	U11	-	-
F1_DQS	T14	K12	-
F1_DQS#	U14	-	-
F2_DQS	R17	D12	-
F2_DQS#	P17	-	-
F3_DQS	K16	B10	60
F3_DQS#	K17	-	-
F0_RE	T10	-	-
F0_RE#/ F0_W/R#	U10	K8	41
F1_RE	T13	-	-
F1_RE#/ F1_W/R#	U13	H10	-
F2_RE	U17	-	-
F2_RE#/ F2_W/R#	T17	F10	-
F3_RE	L17	-	-
F3_RE#/ F3_W/R#	L16	B7	59
F0_WE#/ F0_CLK	T9	K7	34
F1_WE#/ F1_CLK	U12	J10	-
F2_WE#/ F2_CLK	T15	G10	-
F3_WE#/ F3_CLK	M17	A8	53
FSH_WP#	P9	H6	30
FSH_R/B#	N10	J7	31

Signal Name	TFBGA 288	TFBGA 144	QFN 88
RX0_P	A6	A5	71
RX0_N	A5	A4	72
TX0_P	A3	A2	74
TX0_N	A2	A1	76
VCCK	B4, B7, C6, C7, D5, D6, D7, E5, E6, E7, E8, E9	C6, C7, C8, C9, D8, D9, E9	5, 26, 27, 47, 49, 51, 67, 68
VCCGQ	H1, H2	G1	18
PHY_VP	C5	B3[1]	69
PHY_VPTX	C4	-	75
PHY_VPH	C2, C3	C2	78
RESREF	B1	C1	79
VCCFQ	K12, K13, L11, L12, M6, M7, M8, M9, M10, M11, M12, N13	F9, G9, H8, H9, J8, J9	36, 43, 48, 55, 61
FSH_VREF	M16	-	-
V12A_PAD	C1, D1	D1	80
VCCAH	D4, E4	D2	82
CRY_VDD33	F3	E2	85
VDTF_VIN	E3	D3	81
VCC_5V	G1	C3	83
V18_PAD	D2, D3	-	-
CGND	G5, G6, G7, G8, G9, H6, H7, H8, H9, H10, J8, J9, L5	D6, D7, E6, E7, F6, G6	66
VSSFQ	D16, F12, F13, F14, G10, G11, G12, H11, H12, J6, J7, J10, J11, J12, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10	E8, F7, F8, G7, G8, H7	-
CRY_VSS33	G2	E3	88
VGNDA	F2	B1	84
PHY_GD	A4, A7, B2, B3, B5, B6	A3, A6, B2, B4, B5	70, 73, 77

Note[1]: The PHY_VP signal shares the same pin with PHY_VPTX in the TFBGA 144 package.

Signal Name	TFBGA 288	TFBGA 144	QFN 88
J_TRST#	M4	J5	19
J_TMS	N4	K4	21
J_TDI	R2	J6	22
J_TDO	L3	K5	23
J_TCK	P2	J4	20
SPI_CS#	L2	-	-
SPI_CLK	K3	J2	-
SPI_MISO	M2	J3	-
SPI_MOSI	L4	-	-
I^2C_SCL	M5	-	-
I^2C_SDA	N2	-	-
GPIO0[0]	U1	-	-
GPIO0[1]	K5	J1	17
GPIO1[0]	R1	G5	11
GPIO1[1]	H5	H1	12
GPIO1[2]	J3	H2	13
GPIO1[3]	J4	H3	14
GPIO1[4]	K2	H4	16
GPIO1[5]	J5	H5	15
GPIO1[6]	T1	-	-
GPIO1[7]	K4	-	-
GPIO2[0]	G3	E5	-
GPIO2[2]	K1	F3	6
GPIO2[3]	H3	F4	7
GPIO2[4]	J2	F5	-
GPIO2[5]	H4	G2	8
GPIO2[6]	L1	G3	9
GPIO2[7]	P1	G4	10
XIN	E1	E1	86
XOUT	F1	F1	87
EXRST#	M1	D5	2
EXCLK	F4	E4	4
TEST0	J1	C4	1
TEST1	N1	C5	-
TEST2	F5	D4	3
NC	A8 - A17, B8 - B17, C8 - C17, D8 - D15, D17, E2, E10 - E17, F6 - F11, F15 - F17, G4, G13 - G17, H13 - H17	F2	-

2.3 Signal Descriptions

The pull-up/down definitions are shown as below.

PU: Internal fixed pull-up

PU[1]: Internal pull-up controlled by firmware

PD: Internal fixed pull-down

PD[1]: Internal pull-down controlled by firmware

Table 2: Flash Interface Signals

Signal	I/O	PU/PD	Description
F0_DQ[7:0]	I/O	-	Flash data bus connected to flash channel 0.
F1_DQ[7:0]	I/O	-	Flash data bus connected to flash channel 1.
F2_DQ[7:0]	I/O	-	Flash data bus connected to flash channel 2.
F3_DQ[7:0]	I/O	-	Flash data bus connected to flash channel 3.
F0_ALE	O	-	Flash address latch enable.
F1_ALE			
F2_ALE			
F3_ALE			
F0_CLE	O	-	Flash command latch enable.
F1_CLE			
F2_CLE			
F3_CLE			
F0_CE0#	O	-	Flash chip enable for flash channel 0.
F0_CE1#			
F0_CE2#			
F0_CE3#			
F0_CE4#			
F0_CE5#			
F0_CE6#			
F0_CE7#			
F1_CE0#	O	-	Flash chip enable for flash channel 1.
F1_CE1#			
F1_CE2#			
F1_CE3#			
F1_CE4#			
F1_CE5#			
F1_CE6#			
F1_CE7#			

Signal	I/O	PU/PD	Description
F2_CE0#	O	-	Flash chip enable for flash channel 2.
F2_CE1#			
F2_CE2#			
F2_CE3#			
F2_CE4#			
F2_CE5#			
F2_CE6#			
F2_CE7#			
F3_CE0#	O	-	Flash chip enable for flash channel 3.
F3_CE1#			
F3_CE2#			
F3_CE3#			
F3_CE4#			
F3_CE5#			
F3_CE6#			
F3_CE7#			
F0_DQS	I/O	-	Fx_DQS/Fx_DQS#: Flash data strobe/Flash data strobe complement. • For SDR access mode, these signals are not used (no connect). • For NV-DDR and Toggle DDR 1.0 access modes, the Fx_DQS indicates the data valid window. Input with read data, output with write data. Edge-aligned with read data, centered in write data. • In NV-DDR2 and Toggle DDR 2.0 access modes, the Fx_DQS indicates the data valid window. Input with read data, output with write data. Edge-aligned with read data, centered in write data. The Fx_DQS is paired with differential signal Fx_DQS# to provide differential pair signaling to the system during reads and writes (e.g., F0_DQS and F0_DQS#).
F0_DQS#			
F1_DQS			
F1_DQS#			
F2_DQS			
F2_DQS#			
F3_DQS			
F3_DQS#			
F0_RE	O	-	Fx_RE/Fx_RE#: Flash read enable/Flash read enable complement. • For SDR access mode, the Fx_RE# enables serial data output. • For NV-DDR2 and Toggle DDR 1.0/2.0 access modes, the Fx_RE# signal is the serial data-out control, and when active, drives the data onto the DQ buses. Data is valid after tDQSRE of rising edge and falling edge of Fx_RE#, which also increments the internal column address counter by each one. The read enable Fx_RE is paired with differential signal Fx_RE# (only in NV-DDR2 and Toggle DDR 2.0 modes) to provide differential pair signaling to the system during reads. Fx_W/R#: Write/read direction control • For NV-DDR access mode, when this signal is latched high, the controller is driving the DQ bus and DQS (data is being written to the bus). When this signal is latched low, the NAND flash is driving the DQ bus and DQS (data is being read from the bus). (This signal shares the same pin with Fx_RE#.)
F0_RE#/ F0_W/R#			
F1_RE			
F1_RE#/ F1_W/R#			
F2_RE			
F2_RE#/ F2_W/R#			
F3_RE			
F3_RE#/ F3_W/R#			

Signal	I/O	PU/PD	Description
F0_WE#/ F0_CLK	O	-	Fx_WE#: Flash write enable. • For SDR access mode, the write enable signal controls the latching of output data. Data, commands, and addresses are latched on the rising edge of Fx_WE#. • For NV-DDR2 and Toggle DDR 1.0/2.0 access modes, this signal controls writes to the DQ bus. Commands and addresses are latched on the rising edge of the WE pulse. Fx_CLK: Clock. • For NV-DDR access mode, this signal is used as the clock. (This signal shares the same pin with Fx_WE#.)
F1_WE#/ F1_CLK	O	-	
F2_WE#/ F2_CLK	O	-	
F3_WE#/ F3_CLK	O	-	
FSH_WP#	O	-	Flash write protect signal directly connected to the flash memory write protect signal.
FSH_R/B#	I	-	Flash ready/busy signals indicating the state, ready or busy of flash memory.

Table 3: SATA Interface Signals

Signal	I/O	PU/PD	Description
RX0_P	I	-	Positive input of receiver differential signal.
RX0_N	I	-	Negative input of receiver differential signal.
TX0_P	O	-	Positive output of transmitter differential signal.
TX0_N	O	-	Negative output of transmitter differential signal.

Table 4: Power Signals

Signal	I/O	PU/PD	Description
VCCK	PWR	-	Power supply 1.2V for core logic.
VCCGQ	PWR	-	Power supply for general I/O.
PHY_VP	PWR	-	Power supply 1.2V for SATA PHY Rx.
PHY_VPTX	PWR	-	Power supply 1.2V for SATA PHY Tx.
PHY_VPH	PWR	-	Power supply 3.3V for SATA PHY.
RESREF	I	-	Reference resistor connection for SATA PHY.
VCCFQ	PWR	-	Power supply 3.3V/1.8V for flash I/O.
FSH_VREF	PWR	-	External flash reference voltage (VCCFQ x 0.5).
V12A_PAD	PWR	-	Analog power supply 1.2V.
VCCAH	PWR	-	Analog power supply 3.3V for regulator.
CRY_VDD33	PWR	-	Analog power supply 3.3V for crystal cell.
VDTF_VIN	PWR	-	Voltage detector input for flash power.
VCC_5V	PWR	-	Voltage detector input for host power.
V18_PAD	PWR	-	Voltage regulator 1.8V output.
CGND	GND	-	Core ground.

Signal	I/O	PU/PD	Description
VSSFQ	GND	-	Ground for GPIO and flash I/O.
CRY_VSS33	GND	-	Analog ground for crystal.
VGNDA	GND	-	Analog ground for regulator.
PHY_GD	GND	-	Analog ground for SATA PHY.

Table 5: Miscellaneous Signals

Signal	I/O	PU/PD	Description
J_TRST#	I	PU	JTAG test reset.
J_TMS	I	PU	JTAG test mode select.
J_TDI	I	PU	JTAG test data input.
J_TDO	O	PD	JTAG test data output.
J_TCK	I	PU	JTAG test clock.
SPI_CS#	O	-	SPI select enable.
SPI_CLK	O	-	SPI clock input.
SPI_MISO	I	-	SPI data input.
SPI_MOSI	O	-	SPI data output.
I^2C_SCL	I/O	PU	I^2C serial bus clock.
I^2C_SDA	I/O	PU	I^2C serial bus data.
GPIO0[0]	I/O	PD[1]	Invert SATA Rx signal (High active).
GPIO0[1]	I/O	PD[1]	Invert SATA Tx signal (High active).
GPIO1[0]	I/O	PU[1]	This signal drives LED indicator for SSD operation. The LED blinks during read/write operations.
GPIO1[1]	I/O	PU[1]	Hardware write protect (Low active).
GPIO1[2]	I/O	PU[1]	This signal drives LED indicator for the SATA link status between the device and the host (supported only in the CFast form factor). This signal can be also used as UART Rx input.
GPIO1[3]	I/O	PU[1]	Force the device to run ROM code (Low active, for debug only). This signal can be also used as UART Tx output.
GPIO1[4]	I/O	PU[1]	DEVSLP (device sleep mode) enable.
GPIO1[5]	I/O	PD[1]	Quick erase control (Low active).
GPIO1[6]	I/O	PD[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO1[7]	I/O	PD[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO2[0]	I/O	PD[1]	Set the driving strength of flash I/O (High active). This setting is low by default.
GPIO2[2]	I/O	PD[1]	NAND flash power supply. "**0**": Supports 3.3V flash memory. "**1**": Supports 1.8V flash memory.
GPIO2[3]	I/O	PD[1]	Toggle NAND configuration. "**0**": Legacy. "**1**": Native Toggle NAND.
GPIO2[4]	I/O	PD[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO2[5]	I/O	PU[1]	This signal determines the operation mode. "**0**": Reliable mode. "**1**": Normal mode (default).
GPIO2[6]	I/O	PU[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO2[7]	I/O	PU[1]	Card detect in.
XIN	I	-	50MHz external crystal input.

Signal	I/O	PU/PD	Description
XOUT	O	-	50MHz external crystal output.
EXRST#	I	PU	External/Test Reset input. Tie high for normal operation.
EXCLK	I	PD	External/Test Clock input. Tie low for normal operation.
TEST0	I	PD	Test signal. Tie to ground for normal operation.
TEST1	I	PD	Test signal. Tie to ground for normal operation.
TEST2	I	PD	Test signal. Tie to ground for normal operation.
NC	-	-	No Connect.

3. Electrical Characteristics

3.1 DC Characteristics

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power Supply	VCCK	1.08	1.2	1.32	V
I/O Pad Power Supply	VCCGQ	1.7	1.8	1.95	V
		2.7	3.3	3.6	V
Flash I/O Power Supply	VCCFQ	1.7	1.8	1.95	V
		2.7	3.3	3.6	V
Flash I/O Reference Voltage	FSH_VREF	0.5 x VCCFQ			V
Analog Power Supply	V12A_PAD	1.08	1.2	1.32	V
	VCCAH	2.7	3.3	3.6	V
	CRY_VDD33	2.7	3.3	3.6	V
SATA PHY Power Supply	PHY_VPH	3.07	3.3	3.63	V
	PHY_VPTX	1.12	1.2	1.32	V
	PHY_VP	1.12	1.2	1.32	V

Table 7: Operating Temperature

Controller Version	Min	Max	Unit
Commercial	0	70	°C
Industrial	-40	+85	°C

Table 8: General DC Characteristics for 3.3V I/O Interface

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage (V_{IO})	VCCGQ	2.7	3.3	3.6	V	
	VCCFQ	2.7	3.3	3.6	V	
High Level Output Voltage	V_{OH}	0.9 x V_{IO}			V	
Low Level Output Voltage	V_{OL}			0.1 x V_{IO}	V	
High Level Input Voltage	V_{IH}		1.65		V	Non-schmitt trigger
		0.8 x V_{IO}		V_{IO} + 0.3	V	Schmitt trigger[1]
Low Level Input Voltage	V_{IL}		1.65		V	Non-schmitt trigger
		V_{SS} - 0.3		0.2 x V_{IO}	V	Schmitt trigger[1]
Pull-up Resistance	R_{PU}	21	70	119	kΩ	
Pull-down Resistance	R_{PD}	21	70	119	kΩ	

Note[1]: Applies to the EXRST# signal.

Table 9: General DC Characteristics for 1.8V I/O Interface

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage (V_{IO})	VCCGQ	1.7	1.8	1.95	V	
	VCCFQ	1.7	1.8	1.95	V	
High Level Output Voltage	V_{OH}	0.9 x V_{IO}			V	
Low Level Output Voltage	V_{OL}			0.1 x V_{IO}	V	
High Level Input Voltage	V_{IH}		0.90		V	Non-schmitt trigger
		0.8 x V_{IO}		V_{IO} + 0.3	V	Schmitt trigger[1]
Low Level Input Voltage	V_{IL}		0.90		V	Non-schmitt trigger
		V_{SS} - 0.3		0.2 x V_{IO}	V	Schmitt trigger[1]
Pull-up Resistance	R_{PU}	47.7	159	270.3	kΩ	
Pull-down Resistance	R_{PD}	44.1	147	249.9	kΩ	

Note[1]: Applies to the EXRST# signal.

Table 10: Power-on Reset

Parameter		Min	Typ	Max	Unit
Detect Voltage	VRR		0.93		V
	VFR		0.76		V
Delay Time	Rise	2.12	2.62	3.27	µs
	Fall	4.06	5.32	6.96	µs

Table 11: Host Voltage Detection

Parameter		Min	Max	Unit
Detect Voltage	VRR		4.14	V
	VFR		4.0	V
Delay Time	Rise	1.5	4.5	µs
	Fall	0.5	1.5	µs

Table 12: Flash Voltage Detection

Parameter		Min	Max	Unit
Detect Voltage (3.3V)	VRR	2.7	2.9	V
	VFR	2.6	2.8	V
Detect Voltage (1.8V)	VRR	1.6	1.8	V
	VFR	1.5	1.7	V
Delay Time	Rise	2.5	3.0	µs
	Fall	0.9	1.5	µs

Table 13: PLL

Parameter	Min	Typ	Max	Unit	Condition
Output Clock	12.5		400	MHz	
Lock-in Time		101.2		µs	
Duty Cycle	45		55	%	
Jitter			10%	UI[1]	
Disable, Power-down Current (1.2V)			1	µA	Regulator Disable
Operating Current (1.2V)			2	mA	f_{CLK} = 400MHz

Note[1]: UI = output frequency.

3.2 Flash Interface AC Characteristics

3.2.1 Legacy NAND (SDR) Interface

Table 14: Flash Interface AC Characteristics for Legacy NAND

Parameter	Symbol	Min	Max	Unit
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	5.0		ns
CLE Setup Time	tCLS	10.0		ns
CLE Hold Time	tCLH	5.0		ns
ALE Setup Time	tALS	10.0		ns
ALE Hold Time	tALH	5.0		ns
Write Cycle Time	tWC	20.0		ns
WE# Pulse Width	tWP	10.0		ns
WE# High Hold Time	tWH	7.0		ns
Write Data Setup Time	tDS	7.0		ns
Write Data Hold Time	tDH	5.0		ns
Read Cycle Time	tRC	20.0		ns
Ready to RE# Low	tRR	20.0		ns
RE# Pulse Width	tRP	10.0		ns
RE# High Hold Time	tREH	7.0		ns

Figure 5: Command Latch Timing

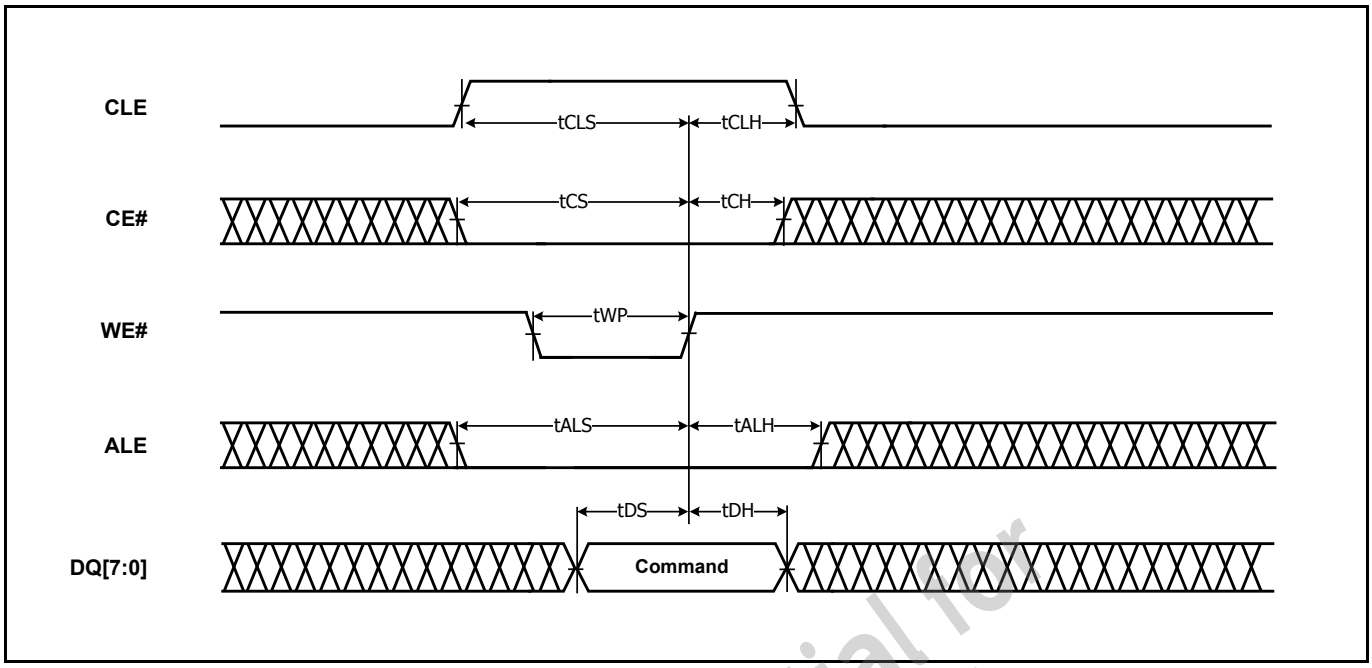


Figure 6: Address Latch Timing

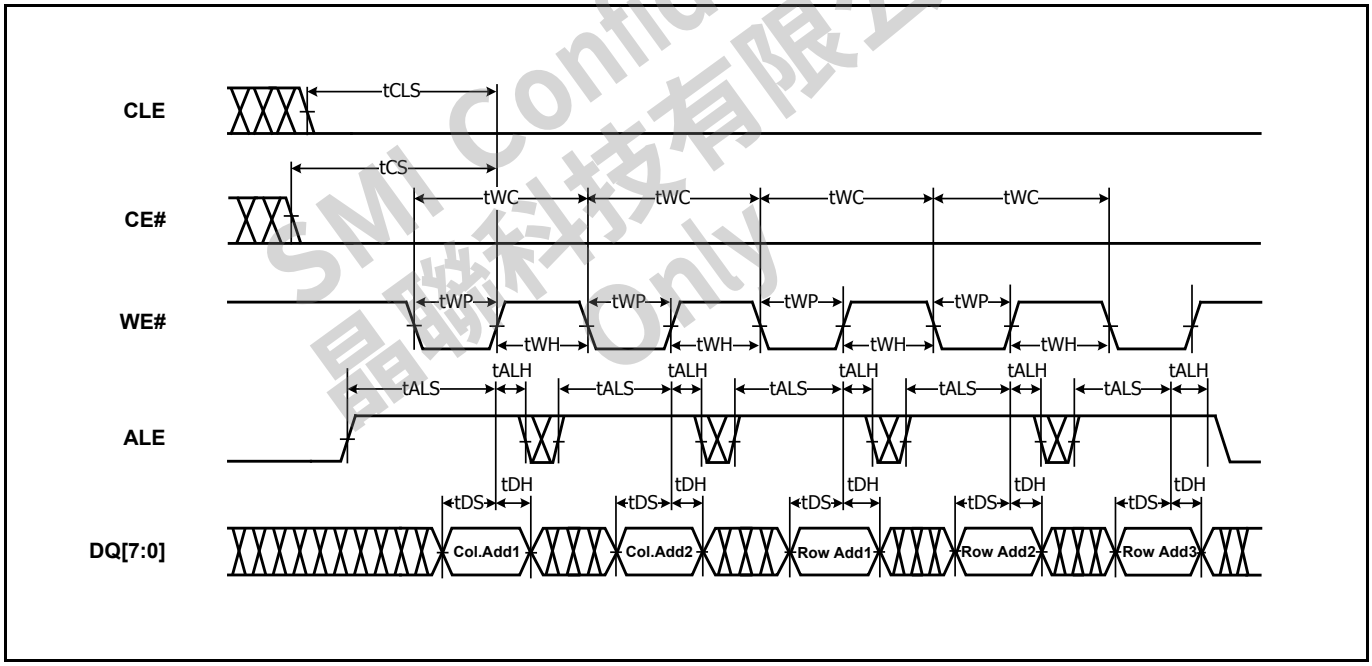


Figure 7: Data Output (Write) Cycle Timing

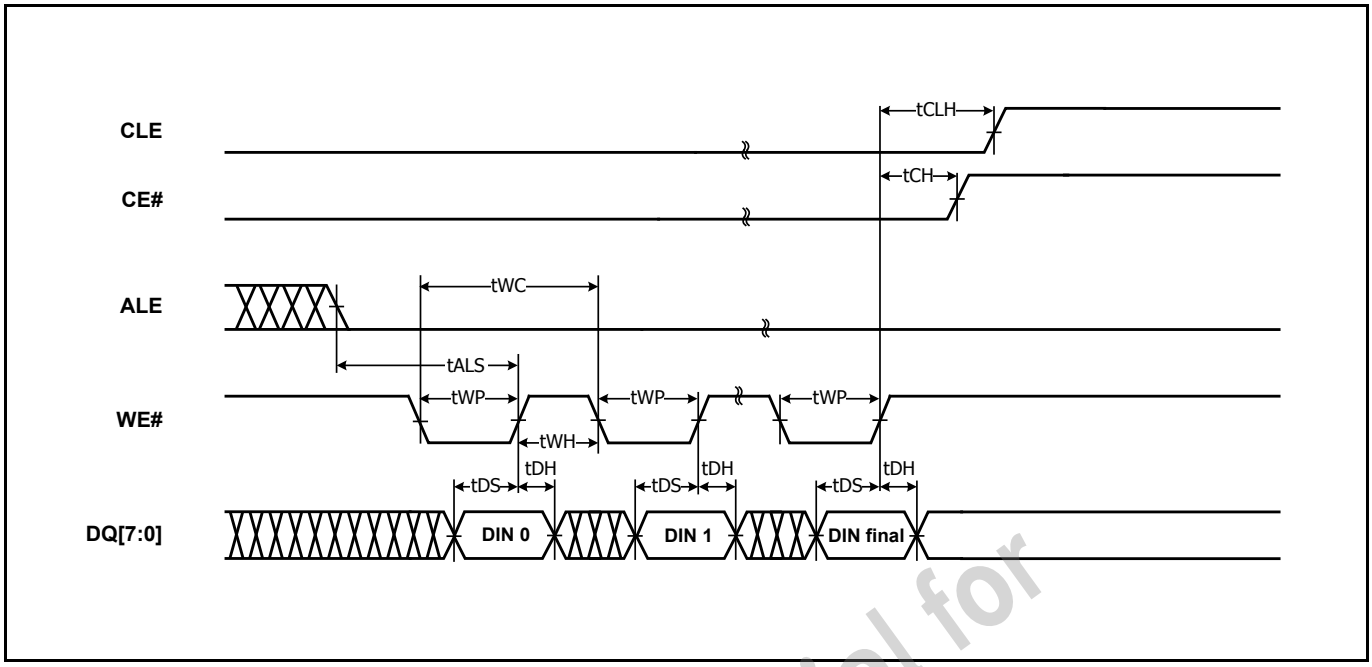
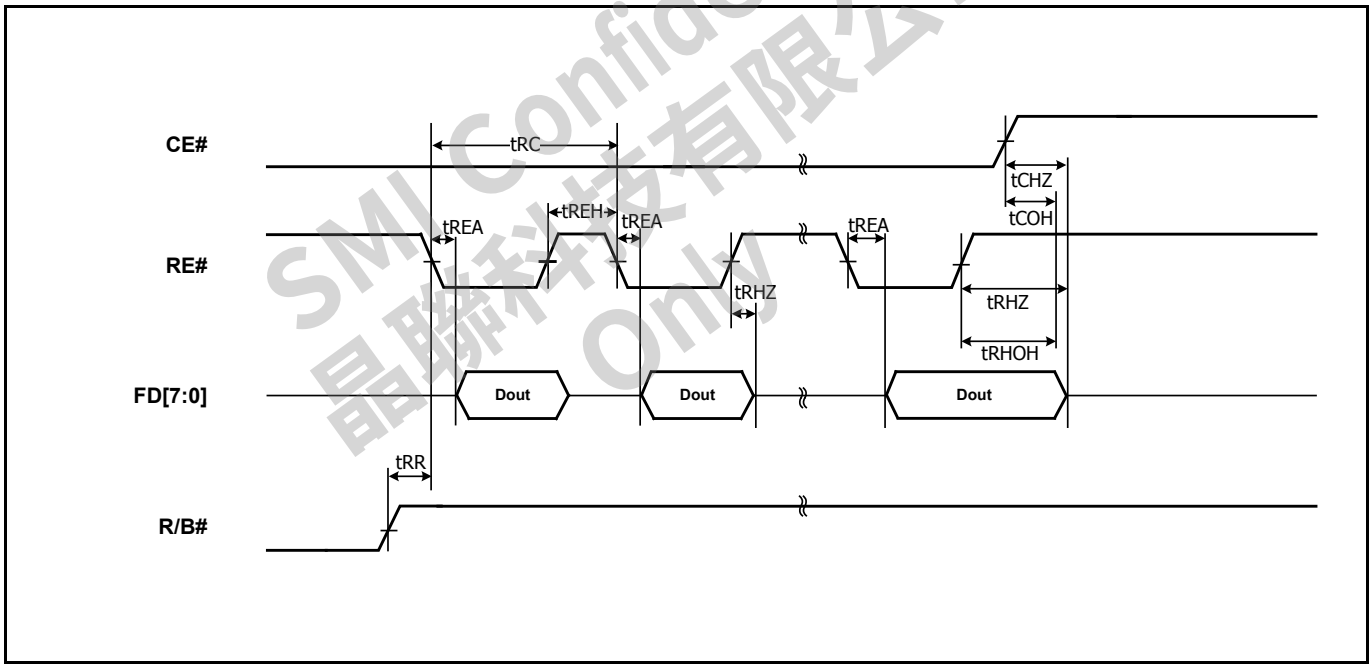


Figure 8: Data Input (Read) Cycle Timing



3.2.2 NV-DDR Interface

Table 15: Flash Interface AC Characteristics for NV-DDR

Parameter	Symbol	Min	Max	Unit
CLK Cycle Time	tCK	10.0		ns
CLK Low Time	tCKL	0.43	0.57	tCK
CLK High Time	tCKH	0.43	0.57	tCK
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	2.0		ns
CLE, ALE, W/R# Setup Time	tCALS	2.0		ns
CLE, ALE, W/R# Hold Time	tCALH	2.0		ns
Command & Address DQ Setup Time	tCAS	2.0		ns
Command & Address DQ Hold Time	tCAH	2.0		ns
Data Output (Write) Setup Time	tDS	0.9		ns
Data Output (Write) Hold Time	tDH	0.9		ns
DQS Falling Edge to CLK Rising Setup Time	tDSS	0.2		tCK
DQS Falling Edge to CLK Rising Hold Time	tDSH	0.2		tCK
DQS Low Pulse Width	tDQSL	0.4	0.6	tCK
DQS High Pulse Width	tDQSH	0.4	0.6	tCK
Data to the 1st DQS Latching Transition	tDQSS	0.75	1.25	tCK
DQS Write Preamble	tWPRE	1.5		tCK
DQS Write Postamble	tWPST	1.5		tCK
W/R# Low To Data Input Cycle	tWRCK	20.0		ns
W/R# Low to DQS/DQ Driven by Flash Memory	tDQSD	0	18.0	ns
Access Window of DQ[7:0] from CLK	tAC	3.0	20.0	ns
Access Window of DQS from CLK	tDQSCK		20.0	ns
DQS-DQ Skew, DQS to Last DQ Valid, Per Access	tDQSQ		0.85	ns
DQ-DQS Hold, DQS to The 1st DQ to Go No-valid	tQH	0.33		tCK
DQ Input Data Valid Window	tDVW	0.24		tCK

Figure 9: NV-DDR Command Cycle Timing

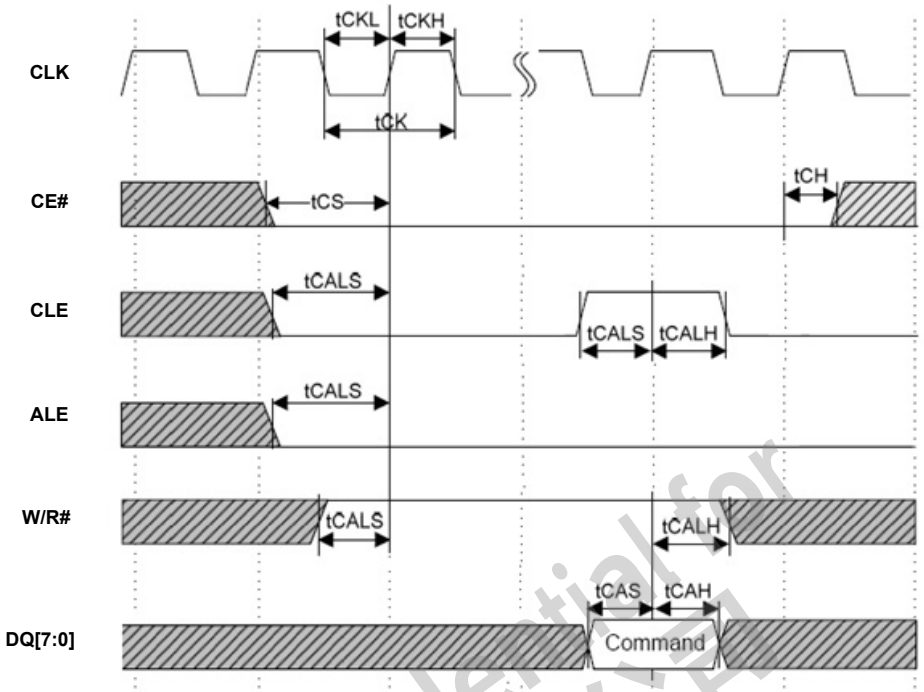


Figure 10: NV-DDR Address Cycle Timing

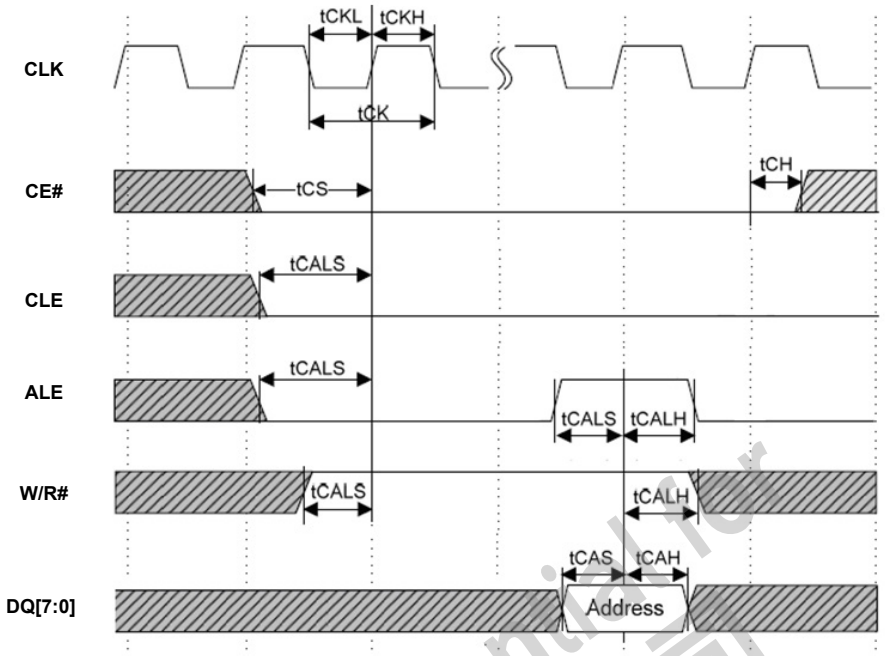


Figure 11: NV-DDR Data Output (Write) Cycle Timing

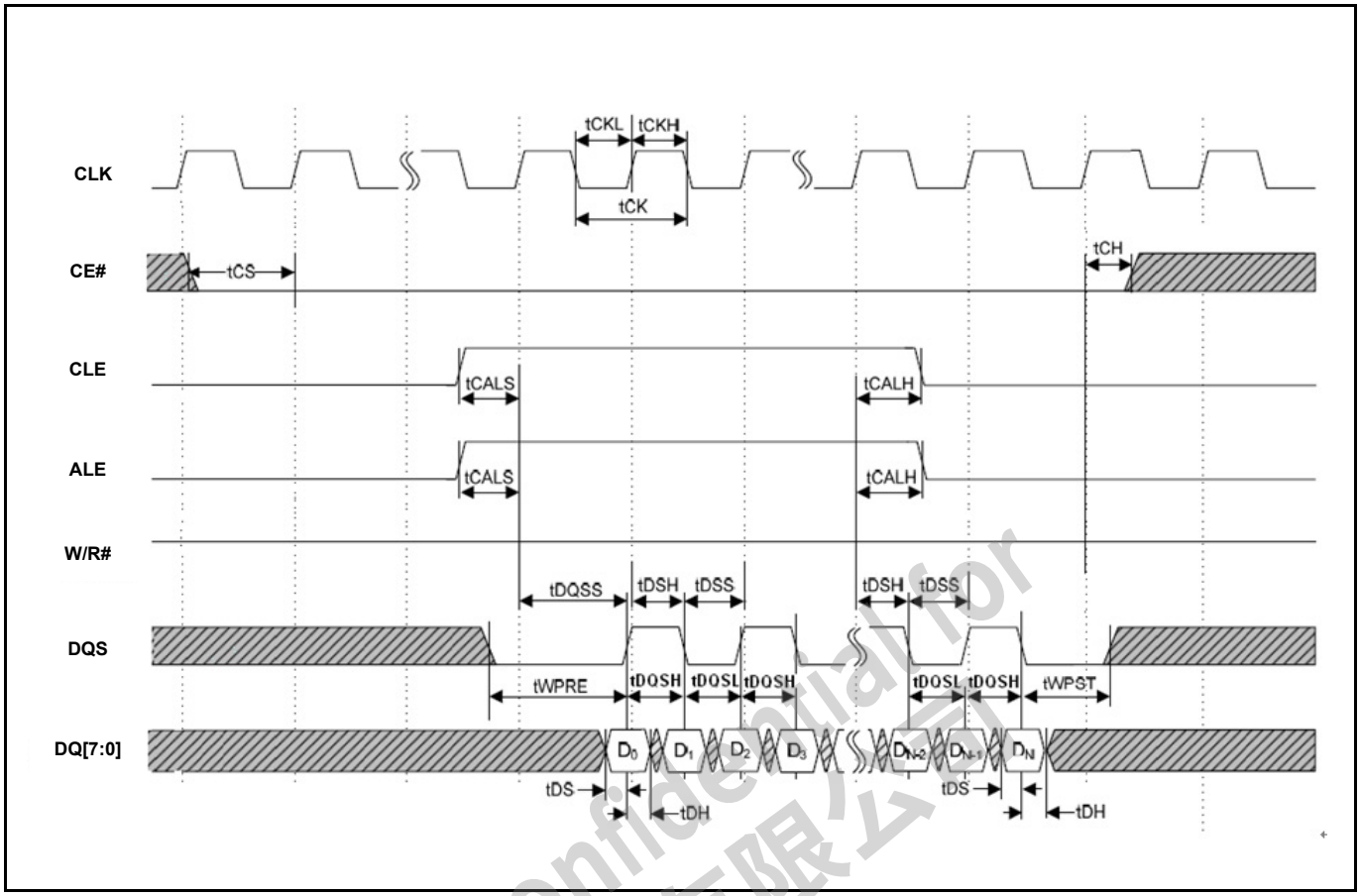
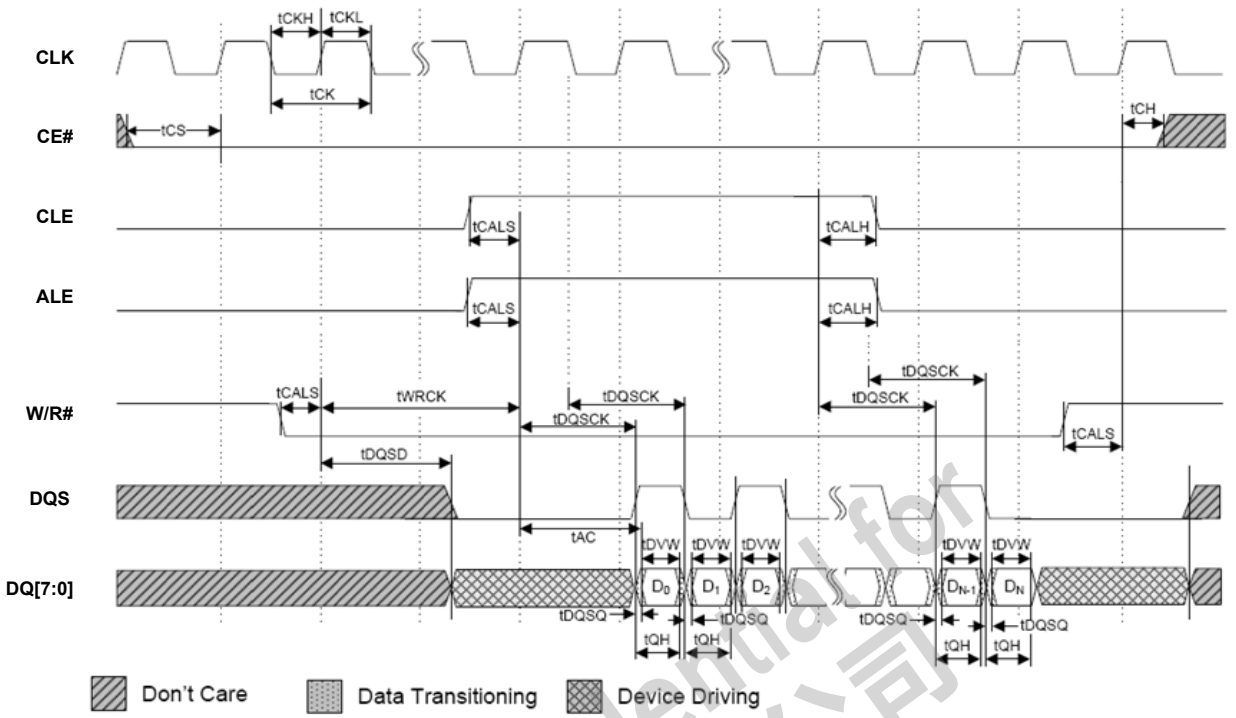


Figure 12: NV-DDR Data Input (Read) Cycle Timing



4. Software Interface

4.1 Command Set

Table 16: Command Set

Command	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out

Command	Code	Protocol
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute OFF-LINE Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-in
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

4.2 Identify Device Information

The Identify Device command enables the host to receive parameter information from the SM2246XT. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in the following table.

4.2.1 Identify Device - SATA

Table 17: Identify Device Data of General SATA Mode

Word	F / V	Default Value	Description
0	F	044Ah	General configuration
1	X	XXXXh	Default number of cylinders
2	V	0000h	Reserved
3	X	00XXh	Default number of heads
4	X	0000h	Obsolete
5	X	0240h	Obsolete
6	F	XXXXh	Default number of sectors per track
7 - 8	V	XXXXh	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	X	0000h	Obsolete
10 - 19	F	XXXXh	Serial number in ASCII (Right justified)
20	X	0002h	Obsolete
21	X	0002h	Obsolete
22	X	0000h	Obsolete
23 - 26	F	XXXXh	Firmware revision in ASCII Big Endian Byte Order in Word
27 - 46	F	XXXXh	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	F	8001h	Maximum number of sectors on Read/Write Multiple command
48	F	0000h	Reserved
49	F	0300h	Capabilities
50	F	0400h	Capabilities
51	F	0200h	PIO data transfer cycle timing mode
52	X	0000h	Obsolete
53	F	0007h	Field validity
54	X	XXXXh	Current numbers of cylinders
55	X	XXXXh	Current numbers of heads
56	X	XXXXh	Current sectors per track
57 - 58	X	XXXXh	Current capacity in sectors (LBAs) (Word 57 = LSW , Word 58 = MSW)
59	F	0101h	Multiple sector setting

Word	F / V	Default Value	Description
60 - 61	F	XXXXh	Total number of user addressable logical sectors for 28-bit commands (DWord)
62	X	0000h	Reserved
63	F	0207h	Multiword DMA transfer Supports MDMA mode 0, 1 and 2
64	F	0003h	Advanced PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	4000h	Additional supported
70 - 74	F	0000h	Reserved
75	F	001Fh	Queue depth
76	F	030Eh	Serial ATA capabilities • Supports Serial ATA Gen3 • Supports Serial ATA Gen2 • Supports Serial ATA Gen1 • Supports Phy event counters log • Supports receipt of host initiated power management requests • Supports Native Command Queuing
77	F	0080h	Serial ATA additional capability • DevSleep_to_ReducedPwerState is supported
78	F	0148h	Serial ATA features supported • Supports Device Sleep • Supports software settings preservation • Device supports initiating power management
79	V	0040h	Reserved
80	F	03FCh	Major version number (ACS-2)
81	F	0000h	Minor version number
82	F	702Bh	Command sets supported 0
83	F	7500h	Command sets supported 1
84	F	4002h	Command sets supported 2
85 - 87	V	XXXXh	Command set/feature enabled
88	V	007Fh	Ultra DMA mode supported and selected
89	F	0003h	Time required for a Normal Erase mode Security Erase Unit command
90	F	0001h	Time required for an Enhanced Erase mode Security Erase Unit command
91	V	0000h	Current advanced power management value
92	V	FFFEh	Master password identifier
93 - 99	V	0000h	Reserved
100 - 103	V	XXXXh	Maximum user LBA for 48-bit address feature set

Word	F / V	Default Value	Description
104	V	0000h	Reserved
105	F	0100h	Maximum number of 512-byte blocks per Data Set Management command
106 - 127	V	0000h	Reserved
128	V	0009h	Security status
129 - 159	X	XXXXh	Vendor specific
160	F	0000h	CFA power mode
161	X	0000h	Reserved
162	F	0000h	Key management schemes supported
163	F	0000h	CF Advanced True IDE Timing mode capability and setting
164 - 168	V	0000h	Reserved
169	F	0001h	Data Set Management supported
170 - 216	V	XXXXh	Reserved
217	F	0001h	Non-rotating media (SSD)
218 - 221	X	0000h	Reserved
222	F	107Fh	Transport major revision (SATA Rev 3.1)
223 - 254	X	0000h	Reserved
255	X	XXXXh	Integrity word

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.

4.2.2 *Identify Device - CFast*

Table 18: Identify Device Data of CFast Mode

Word	F / V	Default Value	Description
0	F	848Ah	General configuration - optional signature for a CFA specification compliant device
1	X	XXXXh	Default number of cylinders
2	V	0000h	Reserved
3	X	00XXh	Default number of heads
4	X	0000h	Obsolete
5	X	0240h	Obsolete
6	F	XXXXh	Default number of sectors per track
7 - 8	V	XXXXh	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	X	0000h	Obsolete
10 - 19	F	XXXXh	Serial number in ASCII (Right justified)
20	X	0002h	Obsolete
21	X	0002h	Obsolete
22	X	0000h	Obsolete
23 - 26	F	XXXXh	Firmware revision in ASCII Big Endian Byte Order in Word
27 - 46	F	XXXXh	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	F	8001h	Maximum number of sectors on Read/Write Multiple command
48	F	0000h	Reserved
49	F	0300h	Capabilities
50	F	0400h	Capabilities
51	F	0200h	PIO data transfer cycle timing mode
52	X	0000h	Obsolete
53	F	0007h	Field validity
54	X	XXXXh	Current numbers of cylinders
55	X	XXXXh	Current numbers of heads
56	X	XXXXh	Current sectors per track
57 - 58	X	XXXXh	Current capacity in sectors (LBAs) (Word 57 = LSW , Word 58 = MSW)
59	F	0101h	Multiple sector setting
60 - 61	F	XXXXh	Total number of user addressable logical sectors for 28-bit commands (DWord)
62	X	0000h	Reserved
63	F	0207h	Multiword DMA transfer Supports MDMA mode 0, 1 and 2

Word	F / V	Default Value	Description
64	F	0003h	Advanced PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	C000h	Additional supported • CFast Specification Support • Deterministic data in trimmed LBA range(s) is supported
70 - 74	F	0000h	Reserved
75	F	001Fh	Queue depth
76	F	030Eh	Serial ATA capabilities • Supports Serial ATA Gen3 • Supports Serial ATA Gen2 • Supports Serial ATA Gen1 • Supports Phy event counters log • Supports receipt of host initiated power management requests • Supports Native Command Queuing
77	F	0080h	Serial ATA additional capability • DevSleep_to_ReducedPwerState is supported
78	F	0148h	Serial ATA features supported • Supports Device Sleep • Supports software settings preservation • Device supports initiating power management
79	V	0X40h	CFast Compliant: • Device Sleep is enabled by setting word 79, bit 8 to one. Enabling and disabling this feature is done using the Set Features command. Serial ATA features enabled • Software Settings Preservation enabled
80	F	03FCh	Major version number (ACS-2)
81	F	0000h	Minor version number
82	F	702Bh	Command sets supported 0
83	F	7400h	Command sets supported 1
84	F	4002h	Command sets supported 2
85 - 87	V	XXXXh	Command set/feature enabled
88	V	007Fh	Ultra DMA mode supported and selected
89	F	0003h	Time required for a Normal Erase mode Security Erase Unit command
90	F	0001h	Time required for an Enhanced Erase mode Security Erase Unit command
91	V	0000h	Current advanced power management value
92	V	FFFEh	Master password identifier
93 - 99	V	0000h	Reserved
100 - 103	V	XXXXh	Maximum user LBA for 48-bit address feature set

Word	F / V	Default Value	Description
104	V	0000h	Reserved
105	F	0001h	Maximum number of 512-byte blocks per Data Set Management command
106 - 127	V	0000h	Reserved
128	V	0009h	Security status
129 - 159	X	XXXXh	Vendor specific
160	F	81F4h	Power requirement - Required for a CFast compliant device that supports Legacy CFA Power Management
161	X	0000h	Reserved
162	F	0000h	Key management schemes supported
163	F	0000h	CF Advanced True IDE Timing mode capability and setting
164 - 168	V	0000h	Reserved
169	F	0001h	Data Set Management supported
170 - 216	V	XXXXh	Reserved
217	F	0001h	Non-rotating media (SSD)
218 - 221	X	0000h	Reserved
222	F	107Fh	Transport major revision (SATA Rev 3.1)
223 - 254	X	0000h	Reserved
255	X	XXXXh	Integrity word

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.

4.3 SMART Feature Set

The SM2246XT supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit.

Table 19: SMART Feature Register Values

Value	Command	Value	Command
D0h	Read Data	D5h	Read Log
D1h	Read Attribute Threshold	D6h	Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

If the reserved size is below the threshold, the status can be read from the Cylinder Register using the Return Status command (DAh).

4.3.1 SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the "Read Data" command (D0h).

Table 20: SMART Data Structure

Byte	F / V	Description
0 - 1	X	Revision code
2 - 361	X	Vendor specific (see 4.3.2)
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 - 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 - 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 - 385	R	Reserved
386 - 395	F	Firmware version/date code
396 - 399	F	Vendor specific
400 - 408	F	'SMI2246XT'
409 - 415	X	Vendor specific
416 - 417	F	Reserved
418 - 419	V	Number of spare block
420	F	Reserved
421 - 422	V	Average erase count
423	F	Reserved
424 - 425	V	Max erase count
426	F	Reserved
427 - 428	V	Min erase count
429 - 510	X	Vendor specific
511	V	Data structure checksum

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.

3. X = content (byte) is vendor specific and may be fixed or variable.
4. R = content (byte) is reserved and shall be zero.

4.3.2 SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

Table 21: SMART Data Vendor-specific Attributes

Attribute ID (hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read error rate
05	LSB	MSB	00	00	00	00	Reallocated sectors count
09	LSB			MSB	00	00	Reserved
0C	LSB			MSB	00	00	Power cycle count
A0	LSB			MSB	00	00	Uncorrectable sector count when read/write
A1	LSB	MSB	00	00	00	00	Number of valid spare block
A2	LSB	MSB	00	00	00	00	Number of cache data block
A3	LSB	MSB	00	00	00	00	Number of initial invalid block
A4	LSB			MSB	00	00	Total erase count
A5	LSB			MSB	00	00	Maximum erase count
A6	LSB			MSB	00	00	Minimum erase count
A7	LSB			MSB	00	00	Average erase count
C0	LSB			MSB	00	00	Power-off retract count
C2	MSB	00	00	00	00	00	Controlled temperature
C3	LSB			MSB	00	00	Hardware ECC recovered
C4	LSB			MSB	00	00	Reallocation event count
C7	LSB	MSB	00	00	00	00	Ultra DMA CRC error count
F1	LSB			MSB	00	00	Total LBAs written (each write unit = 32MB)
F2	LSB			MSB	00	00	Total LBAs read (each read unit = 32MB)

4.4 Capacity

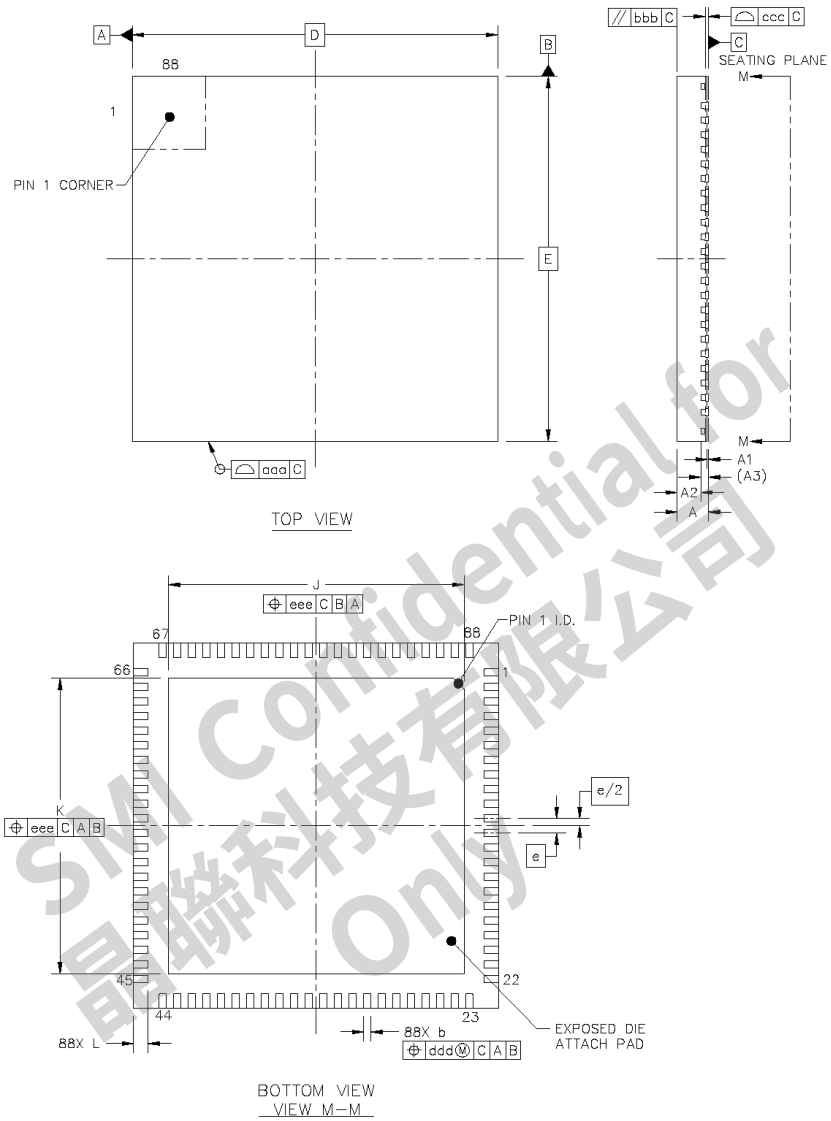
This section depicts the default storage capacity and settings for cylinders, heads, and sectors. Users can change these settings using SMI mass production software.

Table 22: Capacity Information

Capacity	Cylinders	Heads	Sectors	Total Sectors	User Data Size
32GB	16,383	15	63	61,865,984	Depended on file management
64GB	16,383	15	63	123,731,968	
128GB	16,383	15	63	247,463,936	
256GB	16,383	15	63	494,927,872	
512GB	16,383	15	63	989,855,744	
1024GB	16,383	15	63	1,979,711,488	

5. Package Information

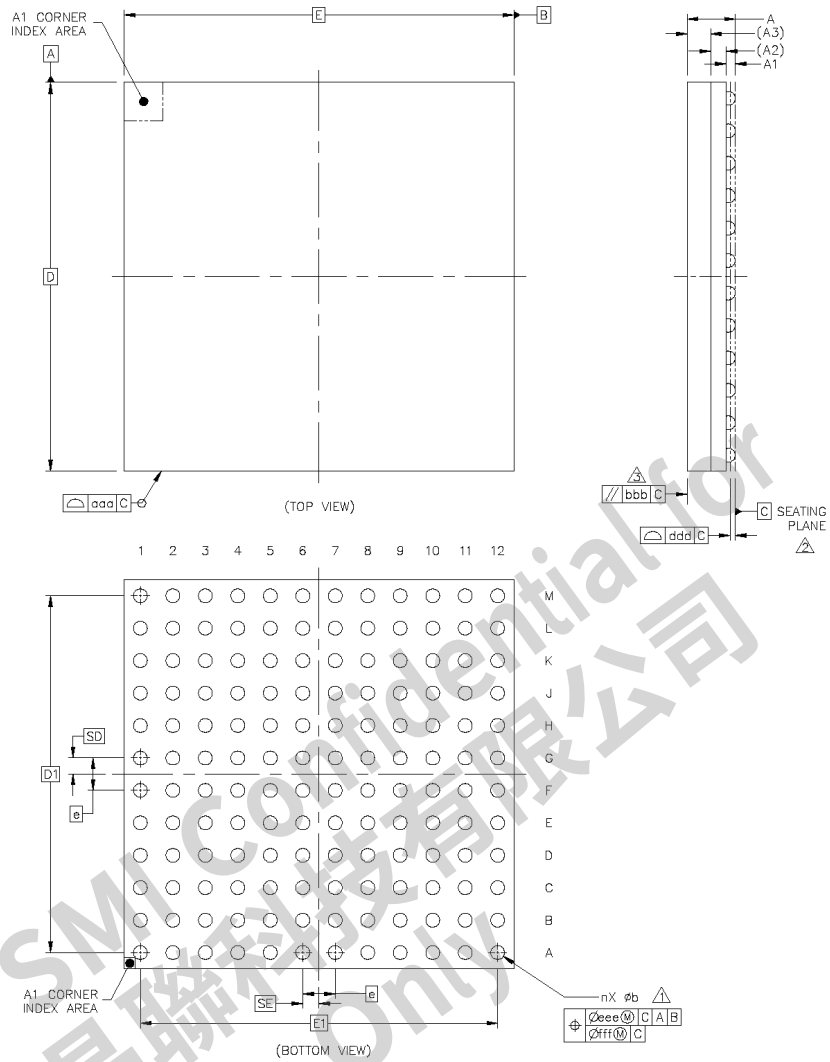
5.1 88-Pin QFN Package



		Symbol	MIN	NOM	MAX			Symbol	MIN	NOM	MAX
Total Thickness		A	0.8	0.85	0.9	EP Size	X	J	8	8.1	8.2
Stand Off		A1	0	0.035	0.05		Y	K	8	8.1	8.2
Mold Thickness		A2	---	0.65	0.67	Lead Length		L	0.35	0.4	0.45
L/F Thickness		A3	0.203 REF			Package Edge Tolerance		aaa	0.1		
Lead Width		b	0.15	0.2	0.25	Mold Flatness		bbb	0.1		
Body Size	X	D	10 BSC			Coplanarity		ccc	0.08		
	Y	E	10 BSC			Lead Offset		ddd	0.1		
Lead Pitch		e	0.4 BSC			Exposed Pad Offset		eee	0.1		

Note: Controlling Dimension: Millimeter. Coplanarity applies to leads, corner leads and die attach pad.

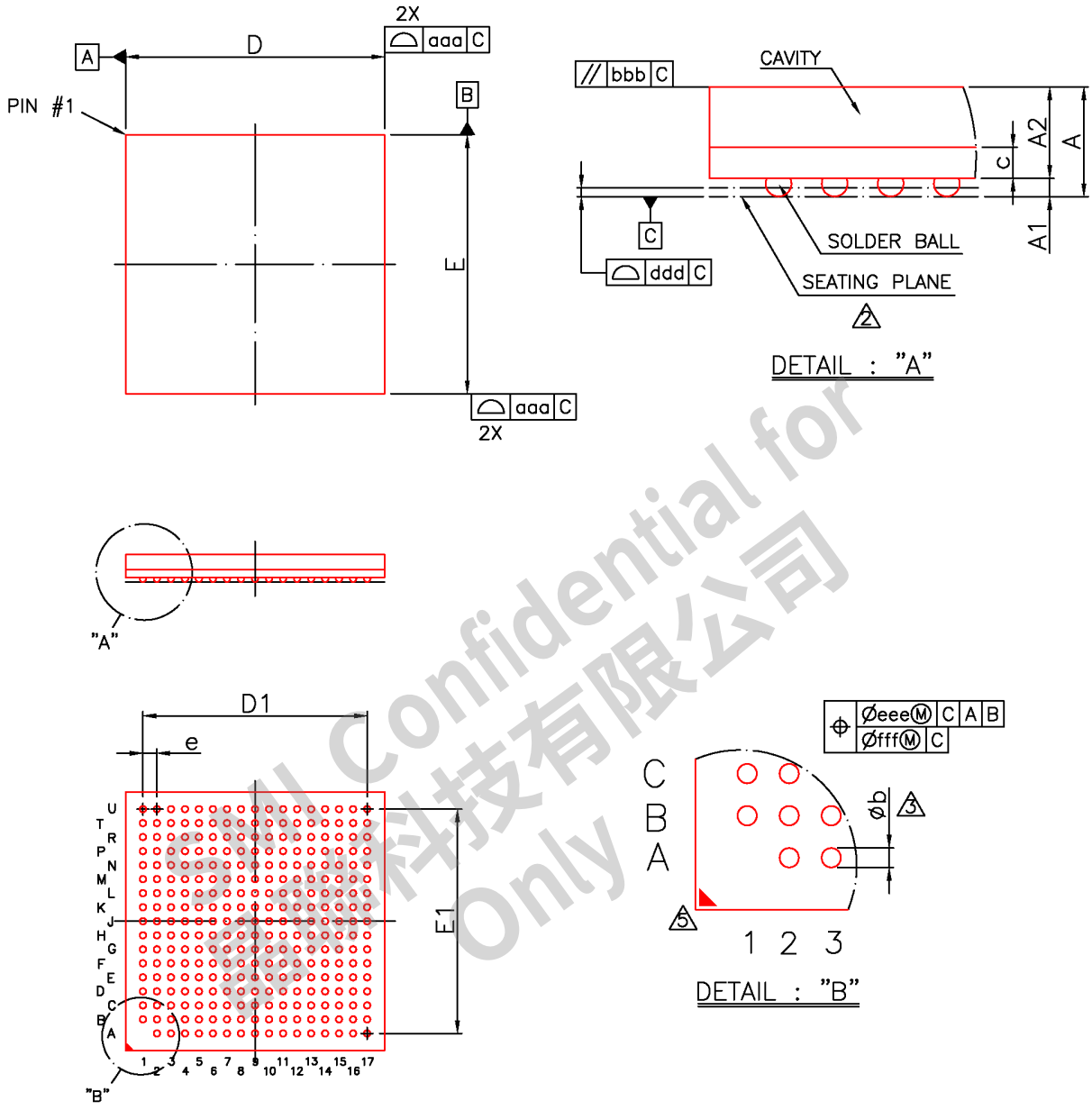
5.2 144-Ball TFBGA Package



	SYMBOL	MIN	NOM	MAX		SYMBOL	MIN	NOM	MAX
Total Thickness	A	---	---	1.2	Ball Count	n		144	
Stand Off	A1	0.16	---	0.26	Edge Ball Center to Center	D1		8.25	BSC
Substrate Thickness	A2		0.36	REF		E1		8.25	BSC
Mold Thickness	A3		0.54	REF	Body Center To Contact Ball	SD		0.375	BSC
Body Size	D		9	BSC		SE		0.375	BSC
	E		9	BSC	Package Edge Tolerance	aaa		0.1	
Ball Diameter			0.3		Mold Flatness	bbb		0.2	
Ball Opening			0.275		Coplanarity	ddd		0.12	
Ball Width	b	0.27	---	0.37	Ball Offset (Package)	eee		0.15	
Ball Pitch	e		0.75	BSC	Ball Offset (Ball)	fff		0.08	

Notes: Controlling dimension: Millimeter.
1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
2. Datum C (seating plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.

5.3 288-Ball TFBGA Package



Symbol	MIN	NOM	MAX	Symbol	MIN	NOM	MAX
A	---	---	1.35	e	---	0.65	---
A1	0.16	0.21	0.25	b	0.25	0.30	0.35
A2	1.01	1.06	1.11	aaa	0.15		
c	0.32	0.36	0.40	bbb	0.10		
D	11.90	12.00	12.10	ddd	0.08		
E	11.90	12.00	12.10	eee	0.15		
D1	---	10.40	---	fff	0.08		
E1	---	10.40	---	MD/ME	17/17		

Notes:
1. Controlling Dimension: Millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: bbb, ddd.
5. The pattern of Pin 1 fiducial is for reference only.

5.4 Top Marking

Figure 13: 88-Pin QFN Top Marking Information

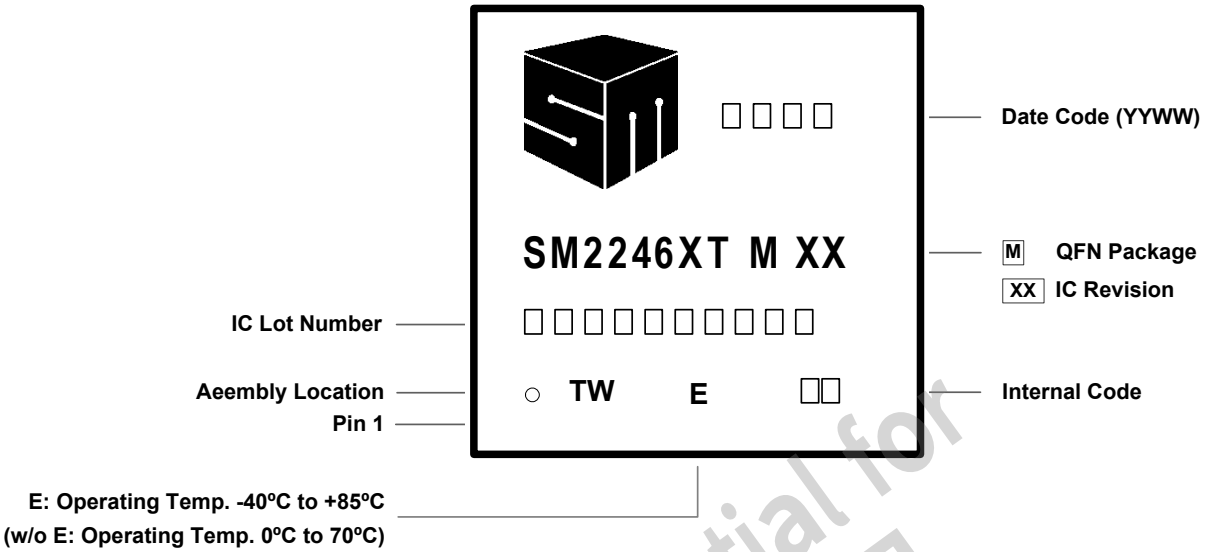


Figure 14: 144-Ball TFBGA Top Marking Information

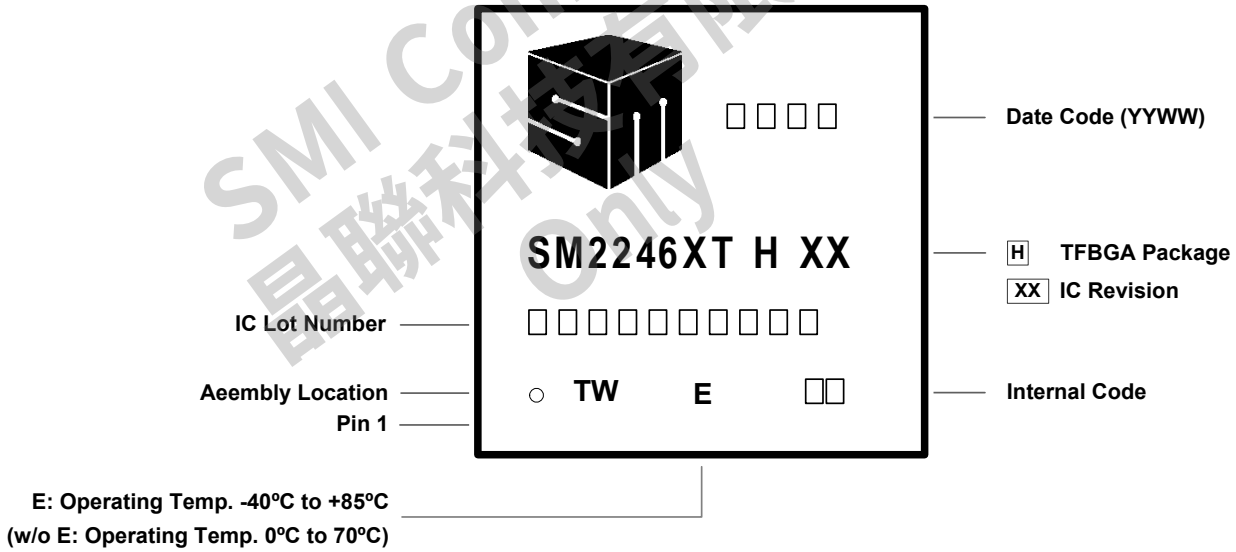
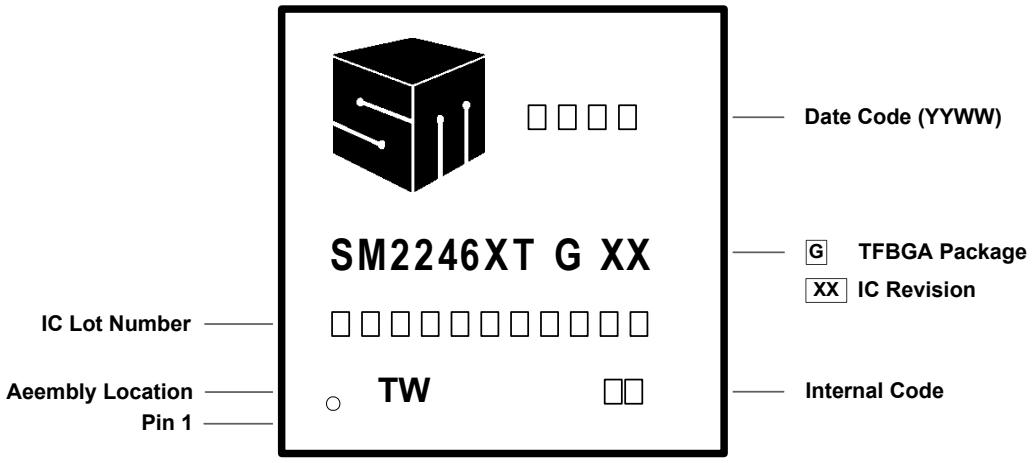


Figure 15: 288-Ball TFBGA Top Marking Information



6. Product Ordering Information

Table 23: Ordering Information

Ordering Number	Operating Temperature	Package Type	Dimensions (mm)
SM224MX0600XT-XX	0°C ~ 70°C	88-pin QFN	10 x 10 x 0.9
SM224ME0600XT-XX	-40°C ~ +85°C	88-pin QFN	10 x 10 x 0.9
SM224HX0600XT-XX	0°C ~ 70°C	144-ball TFBGA	9 x 9 x 1.2 (0.75 pitch)
SM224HE0600XT-XX	-40°C ~ +85°C	144-ball TFBGA	9 x 9 x 1.2 (0.75 pitch)
SM224GX0600XT-XX	0°C ~ 70°C	288-ball TFBGA	12 x 12 x 1.35 (0.65 pitch)

Note: The suffix “XX” denotes the IC revision.