ASMEDIA TECHNOLOGY INC

ASM1352R Datasheet

USB3.1 to Dual SATA Bridge Controller

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	June 13, 2014	Initial Release
0.2	September 29, 2014	Updated General Features Updated Serial SATA features Updated USB features Corrected typo “Mass Storage Class”. Updated RAID mode switch by GUI control in Hydratek Updated Pin Description of RAID mode selection pins, GPIO2, and GPIO8 Updated ESD information Updated PCB design guide under thermal pad Updated power consumption
0.3	October 24, 2014	Updated power consumption Updated SATA port and clock interface pin description

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1. General Description

Engaged in high speed I/O solutions and storage application developments, ASMedia Technology is committed on enlarging product portfolio by introducing USB 3.1 to SATA 6Gbps RAID/Port Multiplier solution. ASM1352R is ASMedia's single chip solution to bridge the USB 3.1 to dual SATA interface. It is highly integrated with ASMedia SuperSpeedPlus, SuperSpeed, and High-Speed and SATA self-designed PHYs. ASM1352R supports one USB 3.1 ports and two SATA device ports, enabling USB PHY up to 10Gbps in compliance with USB 3.1 specifications and enabling Serial ATA PHYs up to 6Gbps high speed interface, following Serial ATA Revision 3.2 Specification.

ASM1352R integrates ASMedia's proprietary **HydraTek** technology, supporting RAID0 (Strip), RAID1 (Mirror), JBOD and Span (BIG) with low power and high efficiency RAID operation, easily configurable modes through GUI, completely free of resource loading on the system CPU. ASM1352R is useful for USB to SATA port expansion and performance boost, not only for internal design but also for external storage application.

2. Features

General Features

- ◇ Integrated 8-bit micro-processor with embedded program RAM and ROM
- ◇ Support SPI NVRAM for Vendor Specific Application of USB Device Controller
- ◇ Support I2C interface with both of master mode and slave mode
- ◇ Support multiple GPIOs for LEDs and Storage Power Control
- ◇ Firmware downloadable by vendor specific commands via SATA host port
- ◇ FAN control support
- ◇ Drive plug-in detection capable
- ◇ Integrated Core power switching regulator
- ◇ Support 3.3V IO power supply and 1.2V Core power supply
- ◇ Support 25MHz with external crystal mode
- ◇ 8mmx8mm 64-pin QFN package
- ◇ Green Package with RoHs Compliance

USB Features

- ◇ Support USB SuperSpeedPlus, USB SuperSpeed, High-Speed, and Full-Speed Operation.
- ◇ Support Mass Storage Class, Bulk-Only Transport Specification Revision 1.3
- ◇ Support Universal Attached SCSI Protocol Specification Revision 1.0
- ◇ Compliant with USB3.1 Specification Revision 1.0
- ◇ Compliant with USB Specification Revision 2.0

Serial ATA Features

- ◇ Serial ATA bus up to 6Gbps Signal bandwidth
- ◇ Serial ATA PHY 1i/1m/1u/2i/2m/2u/3i/3u compliance
- ◇ Support SATA NCQ command
- ◇ Support over 2TB drives
- ◇ Staggered spin-up
- ◇ SATA Partial/Slumber support
- ◇ Power down capable for each storage drive
- ◇ SATA in-band commands support
- ◇ Pass through support for vendor specific commands
- ◇ Compliant with Serial ATA Specification Revision 3.2
- ◇ Support Spread Spectrum Control of USB3.0 and SATA interface to improve the EMI performance
- ◇ Support ATA/ATAPI Packet Command Set
- ◇ Support ATA/ATAPI LBA48 addressing mode

Hydratek Features

- ◇ Support hardware RAID 0/1/JBOD/SPAN (BIG) mode
- ◇ RAID mode switch by hardware strapping
- ◇ Failed or degraded drives detection and report
- ◇ Automatic background rebuilding support

- ◇ Auto recovery from checkpoint location
- ◇ RAID error log
- ◇ SMART drive monitoring

3. Package Type

- ◇ Green Package 8x8 QFN 64L (Pb-free)

4. Functional Diagram

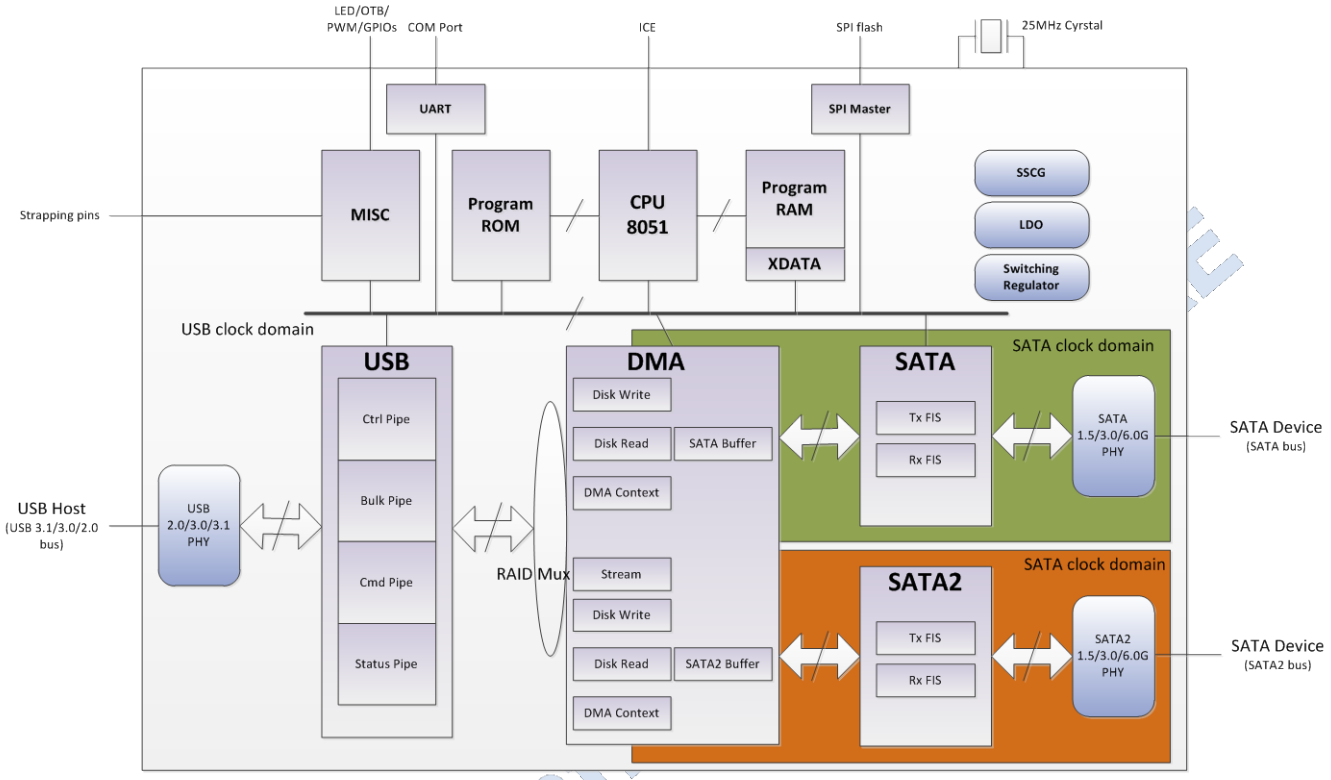


Figure 1: Functional Diagram of ASM1352R

5. Pinout Diagrams

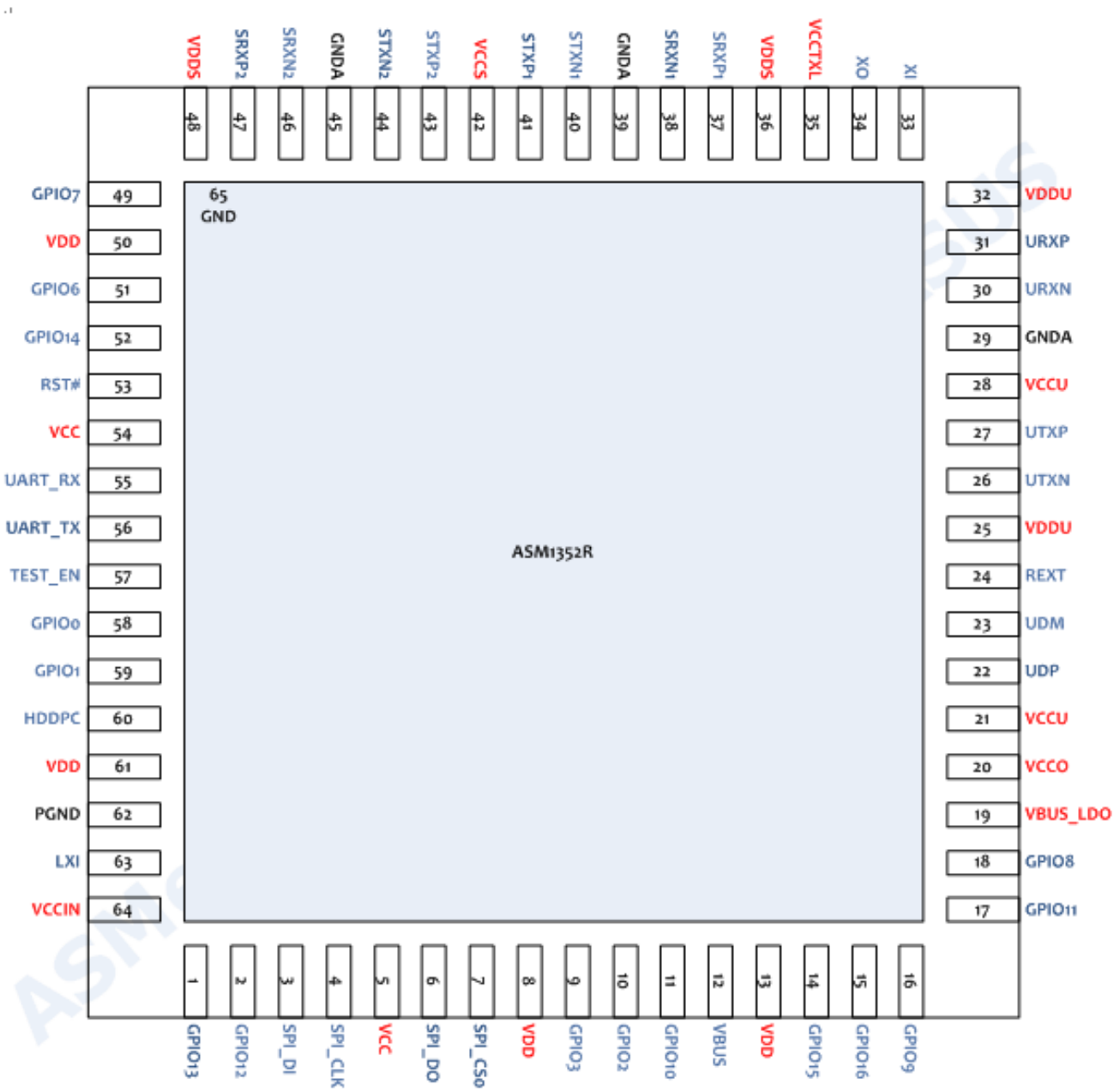


Figure 2: ASM1352R Pinout

6. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin No.	Name	TYPE	Descriptions
USB interface			
23	UDM	DB	USB2.0 negative Data Signal
22	UDP	DB	USB2.0 positive Data Signal
26	UTXN	DO	SuperSpeed USB negative Transmitter Signal
27	UTXP	DO	SuperSpeed USB positive Transmitter Signal
30	URXN	DI	SuperSpeed USB negative Receiver Signal
31	URXP	DI	SuperSpeed USB positive Receiver Signal
SATA interface			
37	SRXP1	DI	SATA positive Receiver Signal for SATA port0
38	SRXN1	DI	SATA negative Receiver Signal SATA port0
40	STXN1	DO	SATA negative Transmitter Signal SATA port0
41	STXP1	DO	SATA positive Transmitter Signal SATA port0
47	SRXP2	DI	SATA positive Receiver Signal for SATA port1
46	SRXN2	DI	SATA negative Receiver Signal SATA port1
44	STXN2	DO	SATA negative Transmitter Signal SATA port1
43	STXP2	DO	SATA positive Transmitter Signal SATA port1
System Signals			
57	TEST_EN	I	Test Enable Signal, with internal pull-down resistor 0: Normal Mode (Default) 1: Test Mode Enable
3	SPI_DI	B	Used as SPI_DI signal. Integrated pull-up resistor.
4	SPI_CLK	B	Used as SPI_CLK signal. Integrated pull-up resistor.
6	SPI_DO	B	General Purpose IO (GPIO5), used as SPI_DO, with internal pull-up resistor.
7	SPI_CS0	B	General Purpose IO (GPIO4), used as SPI_CS0, with internal pull-up resistor.
9	GPIO3	B	General Purpose IO, used as I2C_CLK. Integrated pull-up resistor.
10	GPIO2	B	General Purpose IO, used as SPI_CS1 or LEDP1, with internal pull-up resistor.
49	GPIO7	B	General Purpose IO, used as PWM 5V tolerance output pin for FAN control, configurable as GPIO via updated firmware. Integrated pull-up resistor.
51	GPIO6	B	General Purpose IO, used as I2C_DATA. Error LED for device port2. Integrated pull-up resistor.
2	GPIO12	B	General Purpose IO, used as Error LED for device port1. Integrated pull-up resistor.
55	UART_RX	B	URAT_RX while debug mode, used as General Purpose IO after power on. Integrated pull-up resistor.
56	UART_TX	B	UART_TX while debug mode, used as General Purpose IO after power on. Integrated pull-up resistor.
58	GPIO0	B	General Purpose IO, used as one touch button 2. Integrated pull-up resistor.
59	GPIO1	B	General Purpose IO, used as Active LED for device port2. Integrated pull-up resistor.

Pin No.	Name	TYPE	Descriptions
60	HDDPC	B	HDD power control pin, use as General Purpose IO. Integrated pull-up resistor. 0: Hard Drive Power Off 1: Hard Drive Power On
11	GPIO10	B	General Purpose IO, used as HDD power control pin 2, used as General Purpose IO. Integrated pull-up resistor. 0: Hard Drive Power Off 1: Hard Drive Power On
12	VBUS	I	USB Cable Power Detector
18	GPIO8	B	General Purpose IO, used as Tachometer input for FAN control or ALED1, with internal pull-up resistor.
1	GPIO13	B	General Purpose IO, used as Present detect or device sleep (DEVSLP) for device port1, with internal Pull up resistor
52	GPIO14	B	General Purpose IO, used as Present detect or device sleep (DEVSLP) for device port2, with internal Pull up resistor
14	GPIO15	B	General Purpose IO, used as RAID mode change. Integrated pull-up resistor.
15	GPIO16	B	General Purpose IO, used as RAID mode selection pin 0 (RM_SEL_0). Integrated pull-up resistor.
16	GPIO9	B	General Purpose IO, used as RAID mode selection pin 1 (RM_SEL_1). Integrated pull-up resistor.
17	GPIO11	B	General Purpose IO, used as RAID mode selection pin 2 (RM_SEL_2). Integrated pull-up resistor.
24	REXT	P	External Reference Resistor with 12.1Kohm +/-1%
53	RST#	I	Power Reset pin
Clock Interface			
33	XI	I	Crystal input or Clock input pin
34	XO	O	Crystal output or Clock output pin
35	VCCTXL	P	Power for Crystal and PLL circuit
Voltage Regulator			
19	VBUS_LDO	P	Linear regulator input
20	VCCO	P	Linear regulator output
64	VCCIN	P	Switching regulator input
63	LXI	P	Connect with external inductor
62	PGND	G	Ground for voltage regulator
Power and Ground			
21, 28	VCCU	P	USB high power pin
42	VCCS	P	SATA high power pin
25, 32	VDDU	P	USB low power pin
36, 48	VDDS	P	SATA low power pin
8, 13, 50, 61	VDD	P	Core power
5, 54	VCC	P	IO power
29, 39, 45	GNDA	G	Analog Ground
65	GND	G	the exposed pad connected to common ground on PCB

6.1 Strapping Table

Strapping for RAID Mode Select

RM_SEL0	RM_SEL1	RM_SEL2	Function Description
1	X	X	Controlled by GUI
0	1	1	JBOD (Port Multiplier)
0	1	0	RAID 1
0	0	1	RAID 0
0	0	0	SPAN (BIG)

Notice: All GPIOs do not support 5V tolerance, except UART_RX and FAN_CTRL

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Stressing the below parameters listed over the absolute maximum rating may cause the device permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over these parameters in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal exhibit voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply for VCC	-0.5 ~ VCC+0.5	V
Power Supply for VDD	-0.5 ~ VDD+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

7.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{CC}	IO Power Supply	3.0	3.3	3.6	V
V_{CCU}	USB Analog High Power Supply	3.0	3.3	3.6	V
V_{CCS}	SATA Analog High Power Supply	3.0	3.3	3.6	V
V_{DD}	Core Power Supply		1.2		V
V_{DDU}	USB Analog Low Power Supply		1.2		V
V_{DDS}	SATA Analog Low Power Supply		1.2		V
T_C	Operating Case Temperature	0	25	95	^{0}C
T_J	Operating Junction Temperature	0	25	120	^{0}C
HBM	Human Body mode ESD	+/-2			KV
MM	Machine Mode ESD	+/-200			V

7.3 DC Electrical Characteristics for VBUS pins

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Level	2			V
V_{IL}	Input Low Level			0.8	V
V_{HYS}	Input Hysteresis	0.57	0.6	0.65	mV
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.4		1.8	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	0.85		1.10	V

7.4 DC Electrical Characteristics for GPIO pins

Symbols	Parameter	VCC=3.3V			Units
		Min.	Typ.	Max.	
V_{IH}	Input High Level	2			V
V_{IL}	Input Low Level			0.8	V
V_{HYS}	Input Hysteresis	0.57	0.6	0.65	mV
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.38	1.6	1.8	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	0.89	1.07	1.22	V
R_{UP}	Internal Pull-up resistance while Vin=0V	70	103	143	KΩ
	Internal Pull-up resistance while Vin=VCC/2 V	40	58.2	79.2	KΩ

Symbols	Parameter	VCC=3.3V Min.	Typ.	Max.	Units
R_{DN}	Internal Pull-down resistance while Vin=0V	68	109	158	KΩ
	Internal Pull-down resistance while Vin=VCC/2 V	39	61.7	88	KΩ
I_{IL-UP}	Input pull-up current after Vin is read, Rup is off & Iil < 1uA when VIN=0	21	32	54	mA
	Input pull-up current after Vin is read, Rup is off & Iil < 1uA when VIN=VCC/2	19	28.4	48	mA
I_{IL-DN}	Input pull-down current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC	19	30.2	54	mA
	Input pull-down current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC/2	17	26.8	48	mA

7.5 DC Electrical Characteristics for RST# pins

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Level	2.6			V
V_{IL}	Input Low Level			1.4	V
V_{HYS}	Input Hysteresis	0.218	0.235	0.25	V
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.88		2.58	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	1.65		2.35	V
I_{IL}	Input pull-up leakage current while Vin=0V			1	uA

7.6 External Crystal Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{XTAL}	Frequency		25		MHz
Δf_{XTAL}	Long Term Stability (at 25^0C)	-30		30	ppm
T_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

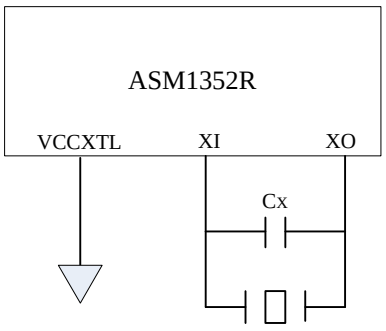


Figure 3: Differential Crystal Design

7.7 Differential Clock Oscillator Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		25		MHz
Δf_{CLK}	Long Term Stability (all condition)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		10		pF
C_{TOTAL}	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R_{TOTAL}	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

7.8 Internal Linear Regular Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{IN_LINEAR}	Input Voltage Range for internal linear regulator	4.5	5	5.5	V
V_{OUT_LINEAR}	Output Voltage Range for internal linear regulator	3.15	3.3	3.45	V
I_{MAX}	Maximum capacity of current output			200	mA

Notice: Please make sure the VCCIN is tied to 5V, even it uses the external 5V to 3.3V regulator.

7.9 Internal Switching Regular Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{IN_SWITCH}	Input Voltage Range for internal switching regulator	3.0		5.5	V
V_{OUT_SWITCH}	Output Voltage Range for internal switching regulator		1.2		V
ΔV_N (p-p)	3.3V input voltage noise/ripple Range	-8		8	%
F_{OSC}	OSC frequency		1.7		MHz
I_{MAX}	Maximum capacity of current output			300	mA
$IP_{(LM)}$	P-channel current limiter		1		A

- **Strong recommendation to have 10uF decoupling capacitor placed close to pin64 to filter the noise/ripple of 3.3V switching regulator input.**

7.10 Power Consumption Characteristics

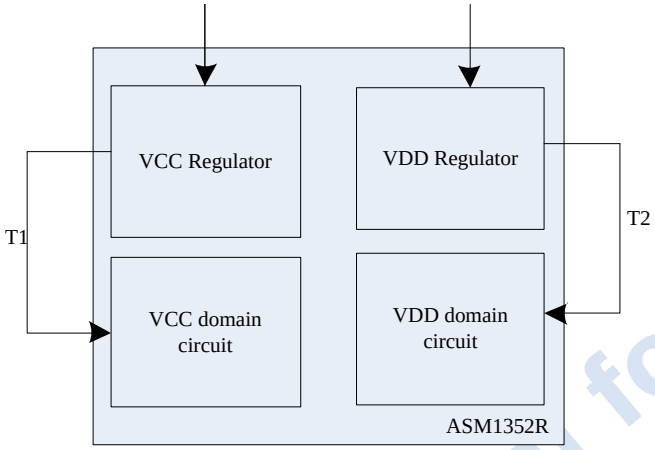


Figure 4: Test point for power consumption

Symbols	Parameter	Condition	USB3.1			USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{VCC}	Total current consumed for 3.3V power domain (Test point T1)	Operating	-	94.61	104		86.37	95		36.78	41	mA
		Idle	-	94.28	104		86.28	95		36.14	41	mA
		Suspend	-	0.72	0.98		0.72	0.98		0.72	0.98	mA
I_{VDD}	Total current consumed for 1.2V power domain (Test point T2)	Operating	-	487.53	537		399.84	440		279.83	308	mA
		Idle	-	343.82	378		320.12	353		273.62	301	mA
		Suspend	-	39.33	43.3		38.73	42.6		38.73	42.6	mA

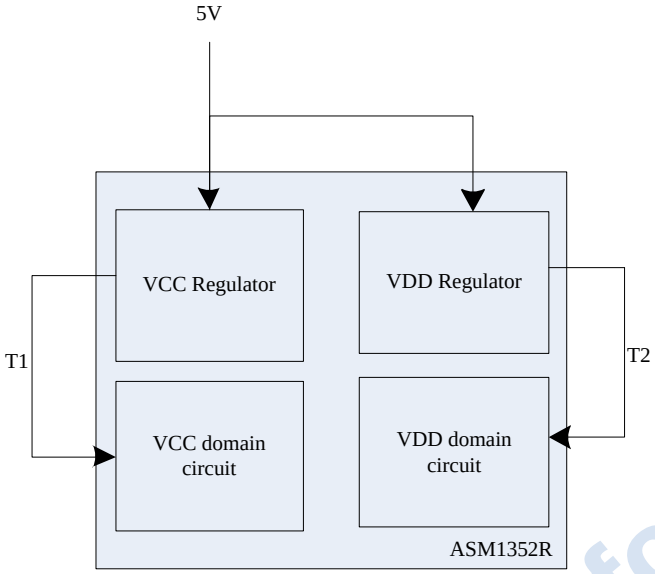


Figure 5: Test point for Type 2

Symbols	Parameter	Condition	USB3.1			USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{VBUS}	Total current consumption for 5V	Operating		255.48	282		217.19	239		122.35	135	mA
		Idle		203.07	224		187.23	206		120.53	133	mA
		Suspend		12.98	14.278		12.98	14.278		12.98	14.278	mA
P_{VBUS}	Total power consumption for 5V	Operating		1277.4	1405		1085.95	1195		611.75	673	mW
		Idle		1015.35	1117		936.15	1030		602.65	663	mW
		Suspend		64.9	72		64.9	72		64.9	72	mW

Notice: Different types of inductors used for internal switching regulator will have varying power consumption figures.

8. Power on Sequence

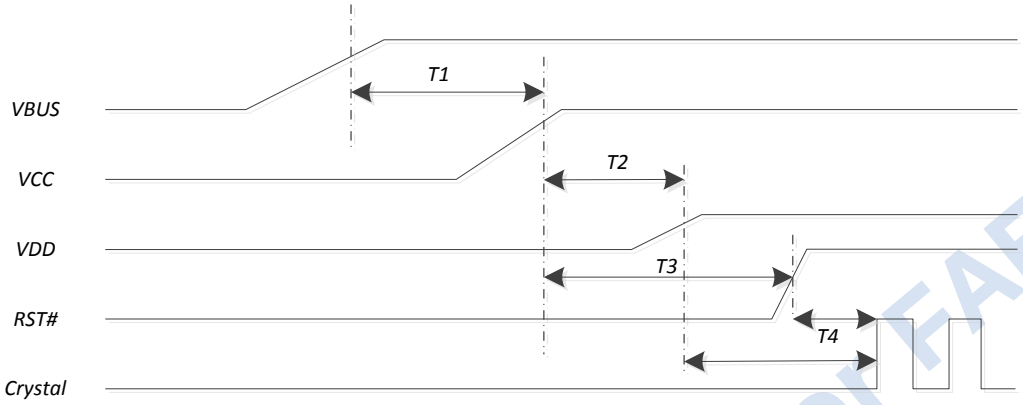


Figure 6: Timing diagram

Symbols	Parameter	Min	Typ	Max	Unit	Remark
T1	The delay of VCC after VBUS is available	0	5	10	ms	Measure from 10% of VCC to 90% of VBUS For Self-powered system or external 5V to VCC regulator, this rule is not needed.
T2	The delay of VDD after VCC is available	N/A		90	ms	Measure from 10% of VCC to 90% of VDD For external VCC to VDD regulator, this rule is not needed.
T3	The delay of RST# after VCC is available	0		N/A	ms	Measure from 90% of RST# to 90% of VCC
T4	The crystal clock is stable after RST# and VDD is available	15	25	40	ms	Measure from 90% of VDD or 2V of RST#
TSLEW	Slew rate of VDD	0		10	ms	Measure from 10% to 90% of VDD

9. PCB Design Guide under Thermal Pad

To improve the thermal efficieny and signal integrity, it is recommended to place the thermal vias under or near to thermal pad. To avoid the process issue, please make sure the thermal via fills with solder covering with solder mask. It is recommended to follow up the pattern on PCB as Figure 8.

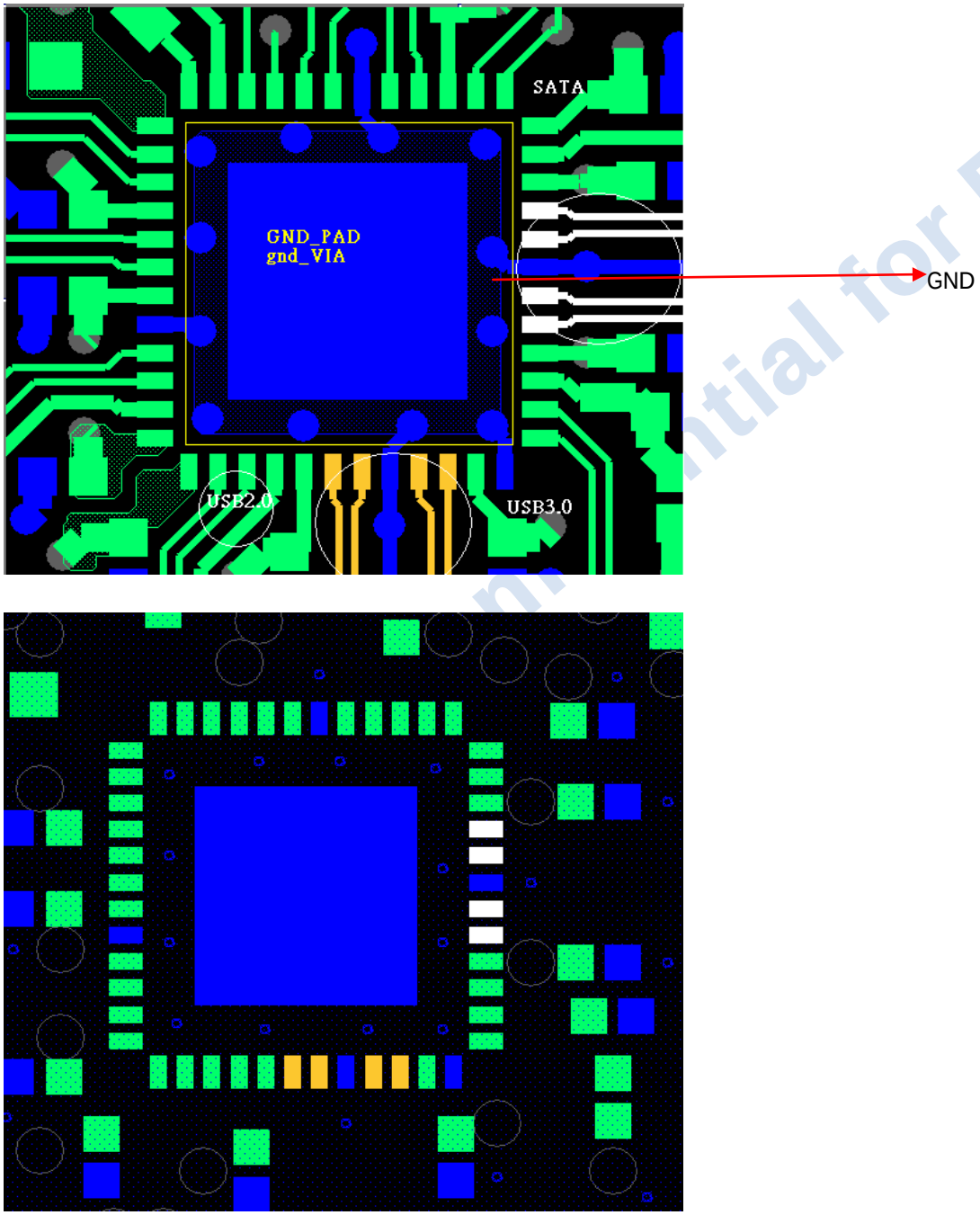
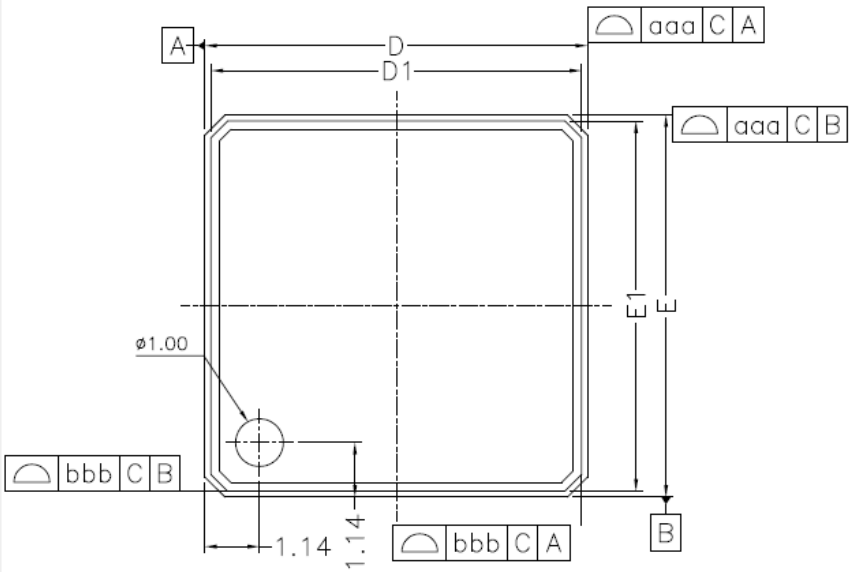
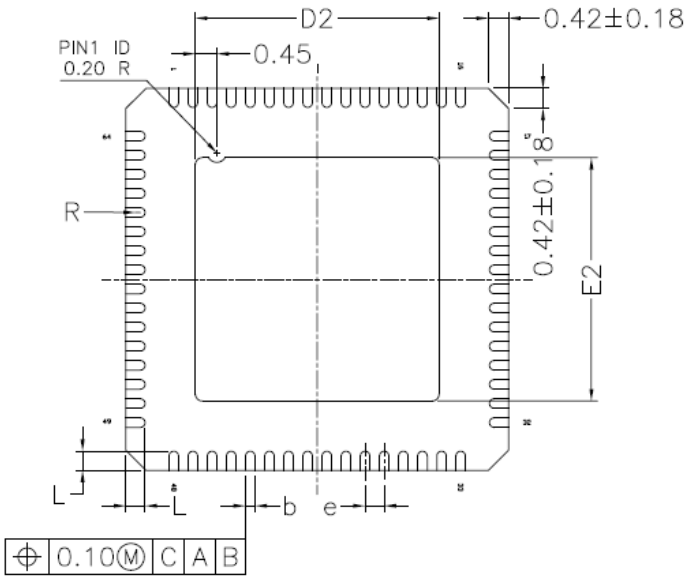


Figure 7: Symbol for via design rule under Thermal pad

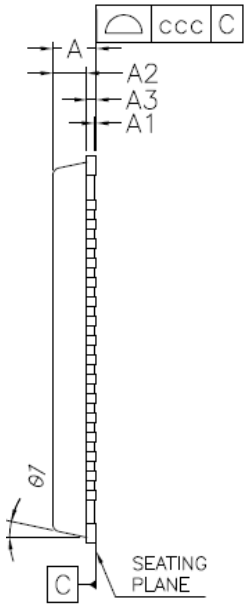
10. Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.31	0.033	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	0.00	0.65	0.70	0.00	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	8.00 bsc			0.315 bsc		
D1	7.75 bsc			0.305 bsc		
D2	4.95	5.10	5.25	0.195	0.201	0.207
E	8.00 bsc			0.315 bsc		
E1	7.75 bsc			0.305 bsc		
E2	4.95	5.10	5.25	0.195	0.201	0.207
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure 8: Mechanical Specification – QFN 64

11. Top Marking Information

TBD