NAND Flash Part Numbering System Micron's part numbering system is available at www.micron.com/support/designsupport/documents/png

		MT	29F	2G	08	Α	Α	Α	Α	Α	WP -	хх	XX	х	ES	:	Α	
Micron Technology																		Design Revision (shrink)
Single-Supply Flash																		Production Status
29F = NAND Flash				_											L			Blank = Production
29E = Enterprise NAND FI	lash																	ES = Engineering Samples
Density																		QS = Qualification Samples MS = Mechanical Sample
1G = 1Gb					1													ms – meenanear sample
2G = 2Gb																		Features
4G = 4Gb 8G = 8Gb																		E = Internal ECC enabled M = Media
16G = 16Gb																		R = FortisFlash features
32G = 32Gb																		S = Security features
64G = 64Gb 128G = 128Gb																		X = Product Longevity Program Z = Polyimide (if applicable)
256G = 256Gb																		,
384G = 384Gb																		Operating Temperature Range*
512G = 512Gb 1T = 1024Gb																		Blank = Commercial (0°C to +70°C) $\Delta \Delta T = \Delta u \text{tomotive Grade } (-40°C \text{ to } +105°C)$
1T2 = 1152Gb																		AIT = Automotive Industrial ($-40^{\circ}C$ to $+85^{\circ}C$)
1HT = 1536Gb																		IT = Extended (-40°C to +85°C) (AKA ET)
2T = 2048Gb 3T = 3072Gb																		WT = Wireless Temp (-25°C to +85°C) *Wafers support only the 0°C to +70°C temperature range
4T = 4096Gb																		waters support only the 0 C to 470 C temperature range
6T = 6144Gb																		Speed Grade
Dovice Width																		Blank = Async only
01 = 1 bit	-				1													10 = 200 MT/s
08 = 8 bits																		6 = 333 MT/s
16 = 16 bits																		5 = 400 MT/s 37 - 533 MT/s
Level																		3 = 667 MT/s
Mark Level																		
A SLC																		Package Code (dimensions in mm)** WP = 48-pin TSOP (CPL version)
E MLC-3																		WC = 48-pin TSOP I (OCPL version)
-																		C5 = 52-pad VLGA, 14 x 18 x 1.0 (SDP/DDP/QDP)
Classification																		G1 = 272-ball VBGA, 14 x 18 x 1.0 (SDP, DDP, 3DP, QDP) G2 = 272-ball TBGA 14 x 18 x 1 3 (ODP 8DP)
Mark Die	nCE	RnB	IO Channels															G6 = 272-ball LBGA, 14 x 18 x 1.5 (16DP)
A 1	0	0	1															H1 = 100-ball VBGA, 12 x 18 x 1.0
B 1 D 2	1	1	1															H2 = 100-ball TBGA, 12 x 18 x 1.2 H3 = 100-ball LBGA, 12 x 18 x 1.4 (8DP)
E 2	2	2	2															H4 = 63-ball VFBGA, 9 x 11 x 1.0
F 2	2	2	1															HC = 63-ball VFBGA, 10.5 x 13 x 1.0
G 3	3	3	3															H6 = 152-ball VBGA, 14 x 18 x 1.0 (SDP, DDP) H7 = 152-ball TBGA_14 x 18 x 1.2 (ODP)
К 4	2	2	2															H8 = 152-ball LBGA, 14 x 18 x 1.4 (8DP)
L 4	4	4	4	1														H9 = 100-ball LBGA, 12 x 18 x 1.6 (16DP)
M 4	4	4	2															J1 = 132-ball VBGA, 12 x 18 x 1.0 (SDP, DDP) I2 = 132-ball TBGA, 12 x 18 x 1.2 (ODP)
R 8	2	2	2	1														J3 = 132-ball LBGA, 12 x 18 x 1.4 (8DP)
T 16	8	4	2	4														J4 = 132-ball VBGA, 12 x 18 x 1.0 (SDP, DDP)
V 16	4	4	4															J5 = 132-Dall IBGA, 12 x 18 x 1.2 (QDP) J6 = 132-ball LBGA, 12 x 18 x 1.4 (8DP)
																		J7 = 152-ball LBGA, 14 x 18 x 1.5 (16DP)
Operating Voltage R		21/ (2 72	2.60\0															J9 = 132-ball LBGA, 12mm x 18mm x 1.5mm (16DP)
$A = V_{CC}$: 3.3V (2.70–3.60V) B = 1.8V (1.70–1.95V)), V _{CCQ} : 3.	3V (2.70	-3.6UV)															^^vvaters are available for some products, please contact Micron for more information
C = V _{CC} : 3.3V (2.70–3.60V)), V _{ccq} : 1.8	8V (1.70-	-1.95V)															All NAND packages are Pb-free.
$E = V_{CC}$: 3.3V (2.70–3.60V)), V _{ccq} : 3.	3V (2.70-	-3.60V) or 1.8V (1.70–1.95V)														had a set of a set
$F = V_{CC}$: 3.3V (2.50–3.60V) G = V_{CC}: 3.3V (2.60–3.60V)), V _{CCQ} : 1.4), V _{CCQ} : 1	2V (1.14- .8V (1.70	-1.26V))–1.95V)							ļ								Mark Interface
H = V _{CC} : 3.3V (2.50-3.60V), V _{ccq} : 1.	2V (1.14	–1.26) or 1.8V (1	.70–1.95V)														A Async only
$J = V_{CC}$: 3.3V (2.50–3.60V)	, V _{ccq} : 1.8	3V (1.70-	-1.95V)															B Sync/Async
$\kappa = v_{CC}$: 3.3V (2.60–3.60V) L = V _{CC} : 3.3V (2.60–3.60V)), V _{CCQ} : 3 , V _{CCO} : 3.3	3v (2.60- 3V (2.60-	-3.60V) or 1.8V (1.70–1.95V)														D SPI
																		Generation Feature Set
																		B = 2nd set of device features (rev only if different than 1st set)
																		C = 3rd set of device features (rev only if different)
																		D = 4th set of device features (rev only if different)
																		ett.

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